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THERMO-MECHANICAL ANALYSIS OF HETEROGENOUS INTEGRATED PACKAGES AND IMMERSION COOLING OF DATA CENTER SERVERS

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THERMO-MECHANICAL ANALYSIS OF HETEROGENOUS INTEGRATED PACKAGES AND IMMERSION COOLING OF DATA CENTER SERVERS

by

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Dedicated to my little sister, the bright shining star Lakshmi Priya Chikalapati, who made the world a better place but left us way too soon

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"Search for perfection, you will find yourself in *Excellence!*"

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Abstract

Thermo-Mechanical Analysis of Heterogenous Integrated Packages and Immersion Cooling of Data Center Servers

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III-V materials such as Gallium Arsenide (GaAs) and Indium Phosphide (InP) are used as substrates for opto-electronic devices like vertical cavity surface emitting lasers (VCSEL), edge emitting lasers and light emitting diodes. System in Package integration of the III-V materials to silicon requires a reliable bonding technique. Though there are several bonding techniques like direct wafer bonding like hetero-epitaxially grown islands on a silicon wafer bonding enable the bonding, flip-chip bonding is used in this study owing to its superior electrical connectivity, mechanical reliability, heat conduction capability and ease of fabrication due to self-alignment.

Finite element models of four different interconnect designs solder balls, flat pads, semi-annular and annular interconnects are studied for their effective thermal dissipation. The efficiency of the proposed designs is studied for mechanical stresses under thermal cycling. CTE mismatch between the GaAs substrate and SiO_2 layers gives rise to mechanical stresses in the interconnects. The models are validated with test vehicles fabricated using standard deposition and lift off processes. The present study aims at understanding the reliability of the indium interconnects in different shapes used to integrate GaAs substrate and silicon on insulator (SOI) wafers.

The high-power density of lasers coupled with the low thermal conductivity of III-V substrates lead to thermal related failures in the devices. Thermal dissipation of the heat generated during laser production is paramount to the proper functioning of the devices. Coupling the III-V substate with SOI wafer gives a proper channel for the heat dissipation and aids in the proper functioning of laser diode.

With the heterogenous integration roadmaps suggesting the saturation of Moore's Law is inevitable, industries are looking at alternatives to pack more functionalities into the electronic packages. As they head towards 3D integration, interposers play a pivotal role in enabling the connections between different chips. Over the last two decades organic and silicon interposers have gained wide popularity and applications, but they are not devoid of limitations. The high cost of silicon interposer and relatively low interconnect density in organic interposer have propelled researchers to look at glass as interposer material. Glass interposers have high electrical resistivity, low cost and low insertion losses. Among a wide variety of glass interposers available, Borosilicate glass interposer with high thermal resistance, optical transmission and high chemical durability, is widely used in the electronic industry, especially in LCD panels owing to its CTE match with silicon and ease of panel-based processing. Copper filled Through Package Vias (TPVs) in glass interposers enable the communication between vertically stacked chips when the lateral communication is taken care of by re-distribution layers. The Coefficient of Thermal Expansion (CTE) mismatch between copper (~ 17.3 ppm/°C) and glass (~ 3.3 ppm/°C) contributes to non-uniform expansion at the interface of TPV and stresses during thermal cycling. The present study aims at using finite-element method to optimize the copper filled through glass via (TGV) or through package via geometry by investigating the stress at critical corners of the interface for different height to diameter ratios of TGV under thermal cycling. The affect of the change in the thickness of the interposer and the diameter of the

via are assessed for various other components of the package configuration such as the solder interconnects connecting the chip and the glass interposer, the solder interconnects connecting glass interposer and the substrate, interfaces of the different chiplets in the package and its affect on the interposer itself.

Submerging a cluster of servers inside a large tank is the customary way of employing single-phase immersion cooling. But this approach requires a complete renovation of existing air cooled infrastructure. A practical approach to converting an air cooled data center to immersion cooled data center can be retaining the rack and server arrangements and supplying each server with immersion liquid in sled configuration, retaining horizontal position. The present study aims at characterizing the thermal performance of a 2-socket server in sled and tank configurations using CFD. In the tank configuration model, the server is immersed vertically with the coolant supply from bottom to top as in the case of typical single-phase immersion deployments. In the sled configuration, the server orientation is retained (horizontally) and the fluid supply is modeled as an inlet and outlet manifold connected to the same side of the server. The CFD modeling approach is aimed to determine the heat transfer behavior of the server in two configurations being looked at was done for a commercially available dielectric immersion liquid, EC 110. A detailed baseline geometry of the server was first simplified, considering only the components that are significant source of heat and/or impact the server flow characteristics. Some of the components considered for analysis include CPU, storage drives and memory modules. The performance of the server in two configurations is compared to determine the efficiency of both the server configurations while ensuring the components do not exceed their respective thermal threshold. Component temperatures are obtained by varying the coolant flow rates and dielectric temperatures.

The thermal conductivity of the immersion cooling liquid plays paramount role in determining the efficiency of the thermal dissipation system. To enhance the thermal properties of the immersion liquid EC110, Al_2O_3 nanoparticles are suspended in the base fluid, making nanofluid. Thermal performance improvements offered by the nanofluid are assessed against the thermal performance and heat dissipation offered by the base fluid.

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Chapter 1

INTRODUCTION

1.1 Motivation

III-V materials like Gallium Arsenide (GaAs), Indium Phosphide (InP) and Gallium Nitiride (GaN) are excellent emitters of light. Various active photonic devices like lasers and light emitting diodes (LEDs) have been demonstrated with varied applications ranging from high power lasers in Watt level output and high speed for Light Detection and Ranging (LiDAR) and 3D sensing devices [1]–[3]. However, they lack the low loss transmission features that silicon possesses. The highly efficient light production devices fabricated from III-V material take advantage of the mature silicon technology for substrates and waveguides[4]–[6]. With the increase in the number of components per chip in photonic chips, the photonic packages are becoming attractive in terms of cost, power consumption and compactness. With their ability to reduce the number of on-chip and off-chip interfaces, they make packages less complex. While there has been extensive exploration of photonic integration in various forms over the past decade, the limited applicability of standard integration platforms due to the mismatch between passive and active devices has restricted their utilization in both military and commercial systems [7].

With improvements in bonding technology, complex photonics circuits that support the functions of sending, receiving, and processing light in an optical system can be achieved. Using low-loss waveguides on silicon, nanosecond-range delays and fast switching are achieved[8], making the circuits even more efficient. Characterizing the bond pads design for thermal, mechanical and electrical performance enables further advances in III-V/Si integration[9].

With the saturation of Moore's law, 2D integration cannot support the performance enhancement of electronic packages. Along with focusing on multiplying the number of transistors per chip area, it is important to explore additional strategies that support enhancement of speed and clock speed in newer electronics. 2.5D and 3D integration attempt to help in the area by increasing the functionality density per chip area[10]. Interposers play a crucial role in enabling 2.5D and 3D integration. Interposers transmit the signal to wider pitches. Organic and silicon interposers have been studied extensively for interposer material. Glass is a new class of material being studied to be employed as an interposer owing to its excellent mechanical properties, compatibility with silicon die and lower costs[10].

Immersion cooling has been gaining popularity as an advanced alternative to the predominantly used air cooling architecture. With the clock speeds and performances enhancements in place, the chips are becoming denser and resulting in more and higher thermal hotspots. To tackle the higher thermal dissipation power, hotspots and achieve uniformity in temperature profile, immersion liquids with higher thermal conductivity are touted as a superior alternative. Yet the usage of immersion fluids in the traditional tank configuration way demands a complete infrastructural makeover of the existing air cooled data centers. The horizontal sled configuration offers a unique solution where the air cooled data centers' infrastructure is retained[11]. The servers are retrofitted with pumps and immersion cooling fluids without changing the initial position, minimizing the costs associated with total infrastructure change. Further, EC110/ Al_2O_3 nanofluid is employed to compare the performance enhancements nanoparticles have to offer in thermal dissipation.

1.2 Overview of Dissertation

The dissertation spans a broad area of working starting from a miniature package design, analysis of the packages thermally and mechanically to concentrating on test vehicle level with analysis on glass interposers and proposing thermal solutions to servers in the form of immersion cooling techniques.

The dissertation can be broadly divided into three subdivisions. The first part spans the study of challenges in co packing of III-V and Silicon materials to realize silicon photonics heterogenous integration. The second part talks about the different interposer materials, their uses and analysis of glass interposer for packaging technology. Third part of the dissertation discusses a server belonging to higher level of packaging being cooled for its hotspots. Immersion cooling technique is used for cooling the server.

Chapter 1 gives the outline, introduction and motivation behind the work done for the dissertation.

Chapter 2 outlines the advancements in silicon photonics and proposes new designs to enable combining III-V/Si substrates. Indium is used to fabricate interconnects that join GaAs and Silicon substrates. Different designs of indium interconnects are proposed and tested for thermal, mechanical and electrical performance. Design modifications are suggested according to results from the three analyses.

Chapter 3 explains the need to alternative advancements to Moore's Law to improve performance and clock speed of the electronic packages without compromising on thermal performance. Glass as a material for interposer is proposed for 3D packaging. Through package via or through glass via geometry is optimized to understand how different packaging co depend on each other in terms of material, geometry and placement.

Chapter 4 discussed the importance of immersion cooling in the modern day data center world. The limitations of air cooling are detailed and the importance and urgent need

for immersion cooling are laid out. Two socket shadow core server from open compute is chosen to understand the immersion cooling improvements on the thermal performance of the server components with heat dissipation. The novelty of the work lies in proposing a new configuration of server placement in horizontal sled configuration whereas the customary way of employing immersion cooling for servers is a tank configuration where the servers are immersed upside down as a cluster in a tank filled with immersion fluid. The feasibility and efficiency of sled configuration are attested against the tank configuration.

Chapter 5 is an extension of chapter 4 where immersion cooling was used for better thermal performance of the servers. Nanofluid is used to take the improvement further. The base fluid is suspended with metal oxide nanoparticle to enhance the thermal properties and thus the thermal performance of the immersed server in the nanofluid.

Chapter 6 concludes the research work on thermal management and reliability ranging from component level to server level. It presents future work and related research improvements.

Chapter 2

CHALLENGES IN CO-PACKAGING OF Si-III/V COMPONENTS IN SILICON PHOTONICS

2.1 Introduction to Silicon Photonics

In the modern semiconductor industry, Silicon Photonics stands at the forefront as an emerging interdisciplinary department that seeks to combine photonics and electronics on a singular silicon substrate. This combination of conventional electronic circuits and the rapid data transmission capabilities of optical communication has attracted substantial attention due to its potential to transform data communication, computing, sensing and more[12].

Silicon photonics attempts to convert electronic signals into optical signals, facilitating data transmission at remarkable velocities. This is achieved by leveraging photonic components such as waveguides, modulators, detectors, and multiplexers all meticulously engineered using conventional silicon fabrication methodologies[13]. The major component in silicon photonics is the silicon waveguide, a small structure that steers light, enabling its propagation with minimal attenuation. Silicon's compatibility with complementary metal-oxide-semiconductor (CMOS) processes expedites the integration of photonic and electronic components on a single chip[14].

Photonics is the branch of engineering that deals with generation detection and manipulation of light. The light is generated using several sources like semiconductors, lasers, LED's, lidars, etc. This generated wave is then carried through mediums like dielectric waveguides, photonic switches and received by detectors and sensors[1].

The main advantage the photonics switches offer is high data transfer capacity. The data can be transferred as fast as the speed of light in the photonic integrated circuits,

in contrast with the CMOS electronics, where the speed of the data is Gbps whereas with a silicon-photonics packages, we can scale it up to terabytes per second[15], [16].

This provides roadmap for the III-V/Si photonic devices and co-packaging architectures while taking advantage of matured Si processing capabilities to enable high density heterogenous integration.

2.1.1 Applications of Silicon Photonics

Silicon Photonics has its application in diverse areas, like automobiles, handheld electronics and smart devices. For example, iPhone has at least 12 to 15 Vertical Cavity Surface Emitting Lasers (VCSELs) in it. Silicon photonics VCSELs are used for purposes like facial recognition, detection and other applications[17]. It also has its applications in automations and manufacturing to enable path and guidance for the moving parts.

In data communication silicon photonics has garnered prominence within data centers and high-performance computing ecosystems, where swift data transmission with minimal energy consumption holds paramount importance. Optical interconnects possess the potential to replace conventional copper-based counterparts by increasing the bandwidth and mitigating latency.

Silicon photonics also has applications in telecommunications such as long-distance communication networks. Optical fibers, with their capacity for communicating for longer distances at a faster pace, combined with silicon photonics enable efficient conversion, routing, and manipulation of optical signals. Silicon photonics-based sensors exhibit highly sensitive, real-time measurements[14]. Applications span from environmental monitoring to healthcare domains, such as real-time glucose monitoring and industrial process optimization.

In autonomous vehicles, lidars are deployed to undertake compact and efficient tasks such as adaptive beam steering, adaptive navigation and signal detection. Lidar also enables high resolution imaging systems for car displays. In quantum computing, silicon photonics offers its applications in enabling the manipulation and conveyance of quantum information[18]–[20].

2.1.2 Direct and Indirect Bandgap Semiconductors Photonics

Semiconductors are a category of material that has electrical conductivity between conductors and insulators. They can be categorized into two broad subdivisions, direct bandgap and indirect bandgap semiconductors.

Semiconductors have valence band and conduction band which determine their electrical and optical properties. The energy difference between the valence band and conduction band is known as bandgap. In the valence band, the electrons are bound to the atoms whereas in the conduction band electrons can move freely and conduct electricity. has its application in diverse areas, like automobiles, handheld electronics and smart devices[8], [21].

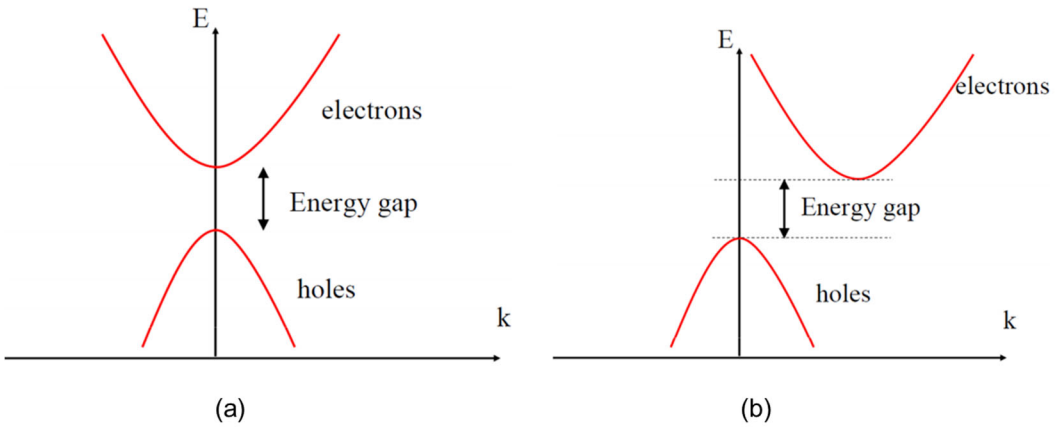


Figure 2-1 Band diagrams of (a) Direct bandgap; and (b) Indirect bandgap semiconductors[22]

As shown in Figure 2-1(a), in the direct bandgap semiconductors, the peak energy of valance band matches with the minimum energy in the conduction band, which creates a path for the electrons to easily move from valance band to conduction band with the emission and absorption of a photon without a change in the momentum.

In other words, semiconductors like Gallium Arsenide (GaAs), Indium Phosphide (InP) and Gallium Nitride (GaN) produce light when an external energy or power is given to these devices, the electron from the holes electron hole pair gets excited and goes to a higher level. When returning to the rest position, the energy is released in the form of light[4].

Direct bandgap semiconductors have efficient light emission capabilities making them an ideal choice for photonic devices like lasers and light emitting diodes (LEDs). Due to the direct transition, the electron-hole recombination when the electrons come back from the excited state, emitting a photon is quicker and efficient giving way for a quicker device operation time[23].

As shown in Figure 2-1(b), in the indirect bandgap semiconductors, the peak energy of valance band does not match with the minimum energy in the conduction band at the same momentum. Thus, a change in momentum is required for the electron to move from valence band to conduction band rendering them inefficient for opto-electronic applications[24].

Silicon is good for photonics, but silicon cannot produce light being indirect bandgap material. The energy is released inside in the form of heat. Silicon may not be good in generating light, but it has an edge with the different properties of it. Especially it's mature processing technology that has been around for decades. The high-volume manufacturing capability, relatively low cost and low loss make it an ideal medium to carry these light waves.

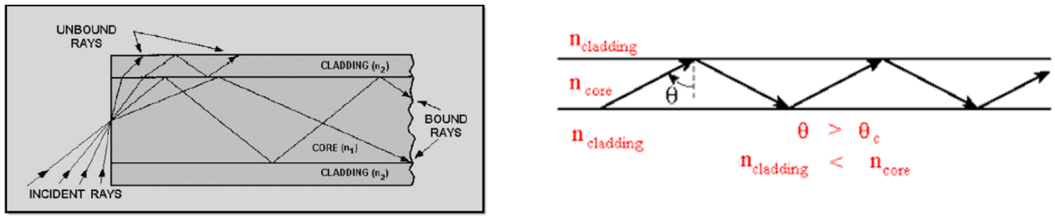
In Silicon Photonics, the direct bandgap material produces the light but owing to their higher optical transmission losses silicon based waveguides and optical switches are used for the light transmission. Taking advantage of the mature silicon technology hybridity integration is employed to combine III-V materials with Silicon to make silicon photonics.

Some of the major draws to silicon photonics are the lower cost per unit area and high crystalline quality of the silicon semiconductor. The relatively high availability of high-quality silicon on insulator (SOI) wafers, where the oxide is etched to make way for silicon waveguide is an additional advantage.

2.1.3 Core and Cladding Layers in Silicon Photonics

From Figure 2-2, the emission comes into a waveguide and then it is found to undergo total internal reflection. When the cladding layer has relatively higher refractive index contrast the total internal reflection is closer to 100% and the losses the light that is

going outside of the core layer and into the cladding layer is less, thus reflecting everything inside and the wave is propagated towards its destination with less losses.



(a) (b)

Figure 2-2 Schematic representation of (a) optical waveguide through clad and core structures; and (b) total internal reflection in optical waveguide[25]

In silicon photonics, all the passive components like the waveguides, couplers, resonators, MUX and De-MUX are fabricated on silicon[5]. Active components like laser and photo detectors that are made from III-V materials on other substrates and later transfer printed or heterogeneously integrated onto silicon resulting in Hybrid Silicon Photonics[26].

2.2 Silicon Photonics Device

Figure 2-3 shows an example of a typical silicon photonics device. On the left side there is a III-V VCSEL which is the light emitting laser source for the package. It is flip chip bonded onto the SOI wafer using solder ball interconnects. The light emitted from the VCSEL comes down to the waveguide layer, where a 45 degree mirror couples it into the silicon waveguide. The silicon waveguide is covered with silicon dioxide cladding layer on all sides. The light is transmitted through the waveguide and the transmission is detected by a photodetector on the right side[27].

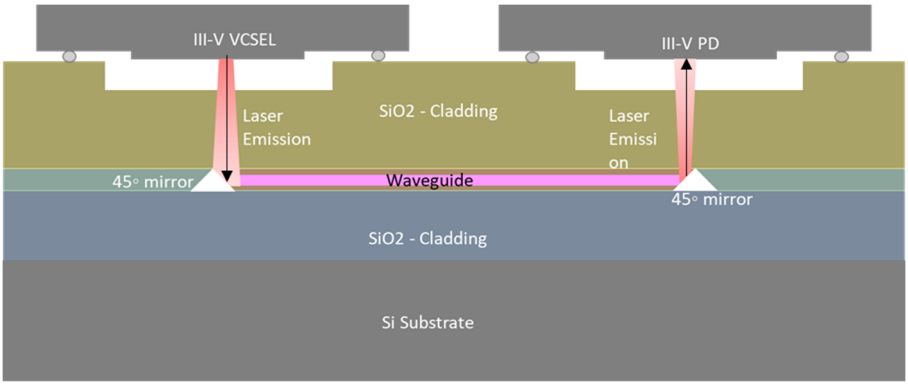


Figure 2-3 Schematic representation of silicon photonics device

Silicon Photonics also has another major draw in the silicon waveguide and silicon dioxide cladding material. The refractive index contrast between the wave guide and the cladding material around it plays a crucial role in the efficient transmission of the light inside the waveguide. The higher difference between the refractive indices of core and cladding layers results in better propagation of light with lower losses.

2.3 Silicon Photonics Hybrid Packages

Figure 2-4 shows another example of silicon photonic circuit. It has a multi-channel array and a base plate, heat sink and Photonic Integrated Circuit (PIC) in it. All of this circuit is mounted on a Printed Circuit Board (PCB).

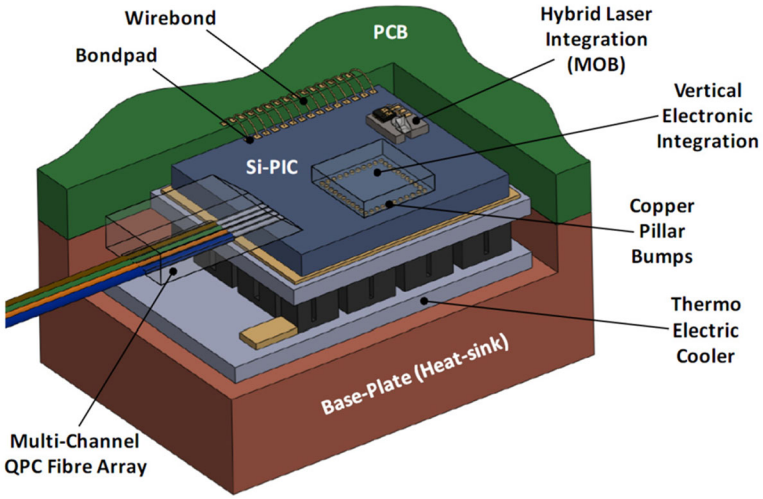


Figure 2-4 Schematic representation of multi-channel photonic integrated circuit packaged with various electronic and optical components[28]

The graph in Figure 2-5 shows number of components increase in the silicon photonics regime mapped out. It is believed that the photonics component increase follows the same path as Moore's Law. Silicon Photonics is also going to grow exponentially. It is just lagging behind electronics by a couple of decades.

Due to the bottlenecks in electrical connectivity and thermal management, the number of silicon photonics components on one chip can only be in the order of thousands[29]. In contrast to the number of transistors on a chip which is in the order of trillions. The current study is about optimizing the interconnect design for both electrical connectivity and thermal management.

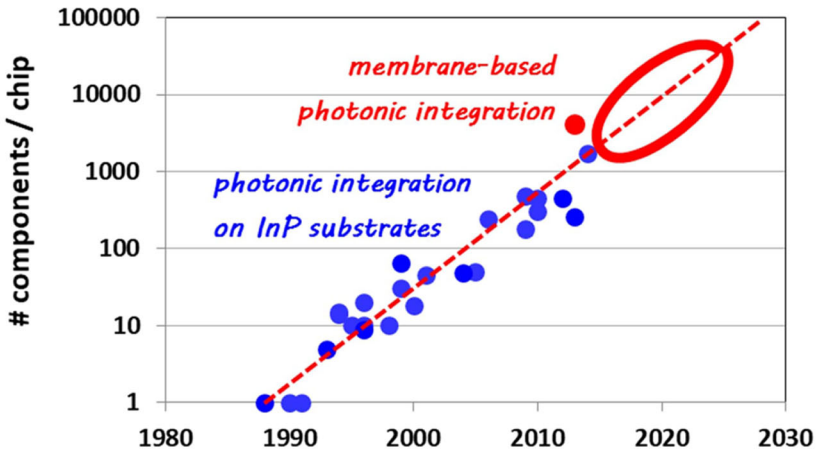


Figure 2-5 Graph showing the historical increment in number of components in photonic integrated circuit[30]

2.3.1 Different Integration Methodologies

Figure 2-6 shows the different approaches in integrating the photonic devices onto the PCB. Monolithic integration is an approach in which a single chip is integrated onto a PCB using wire bonds, then the photonic inflicting is. It can be monolithic, and then the photonic and electronic integrated circuits can be side by side in a 2D integrated fashion using wire bonds or it can go to an advanced packaging level like 2.5D or 3D integration where solder bumps interposers and through package vias are used for the integration. 3D integration can be with the passive interposer as well as an active interposer for photonic integrated circuits.

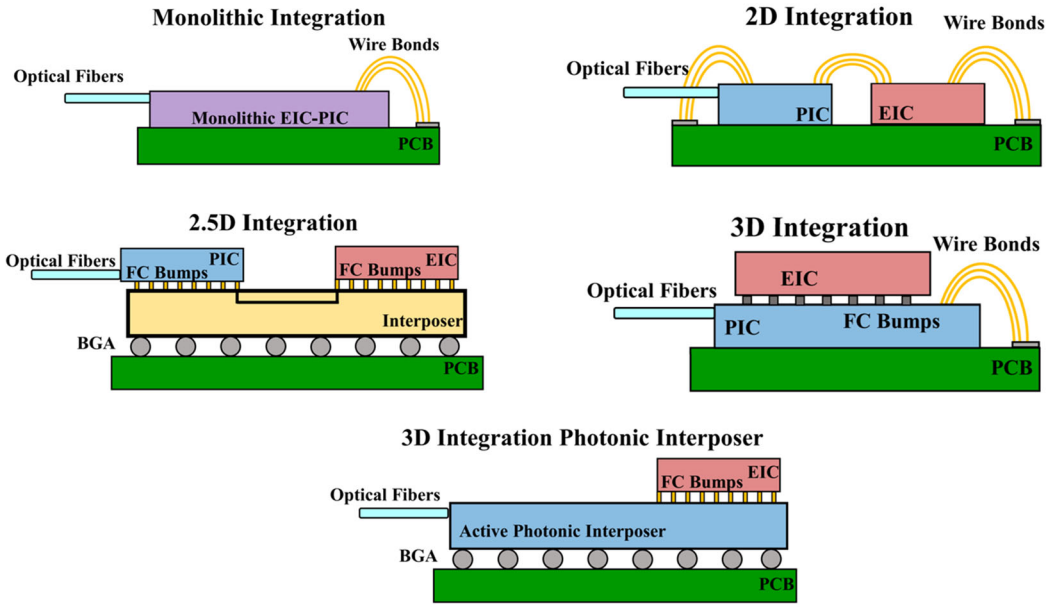


Figure 2-6 Schematic representation of various integration methodologies including monolithic integration, 2D integration, 2.5D integration, 3D integration and 3D integration with photonic interposer[31]

2.3.2 Reliability of Solder Balls in III-V/Si Integrated Circuits

Figure 2-7 shows an example of one of the literature studies where solder balls were used for packaging the III-V substrate and the getting it onto the silicon substrate. Indium solder bumps were used in this study. This study highlights how, under high pressure test, high temperature test and especially thermal cycling test, there are cracks that are developed inside these solder balls.

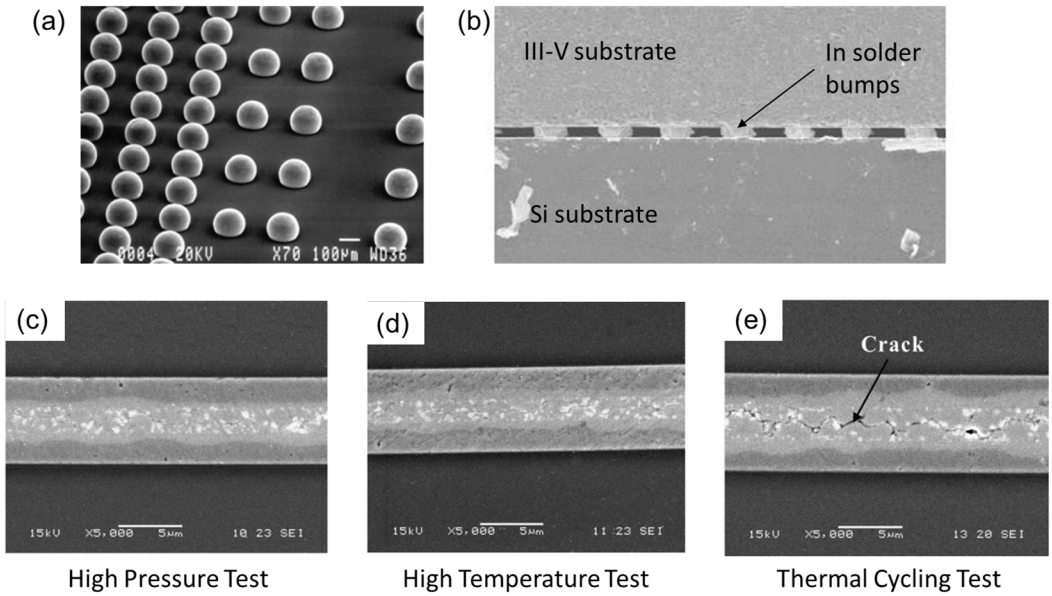
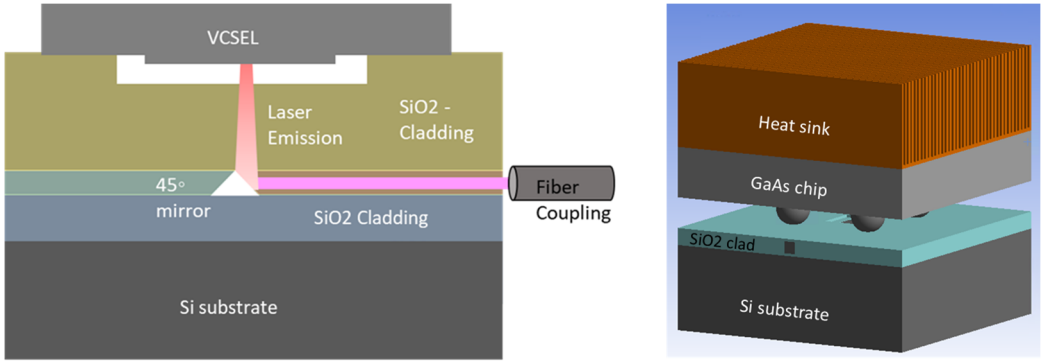


Figure 2-7 Scan electron microscope (SEM) images of (a) indium bumps; (b) III-V/Si indium bump bond interface; zoom-in SEM images at interface (c) after high pressure test; (d) after high temperature test; and (e) after thermal cycling test[32]

2.4 Interconnect Designs for III-V/Si Integration

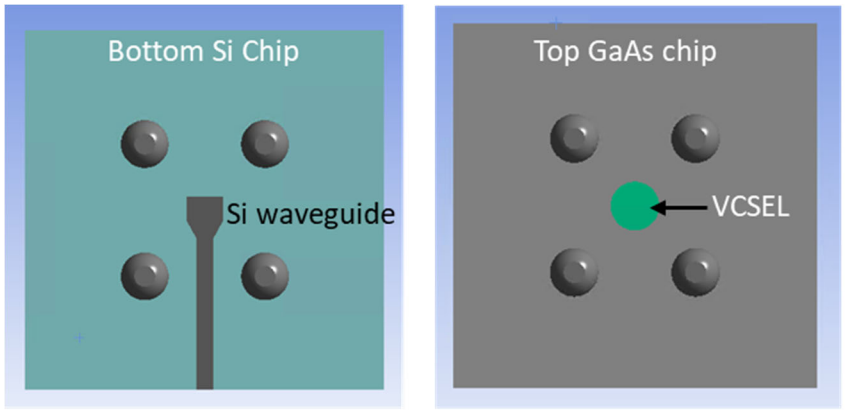
To mitigate the problem of solder joint reliability the present study proposes four different interconnect designs. Figure 2-8(a) shows silicon photonics chiplet design. The bottom of it is a silicon substrate on which there is a silicon dioxide cladding layer as shown in Figure 2-8.



(a) (b)

Figure 2-8 (a) Cross-section schematic of VCSEL-on-Si co-packaging; and (b) 3D model created in Ansys SpaceClaim for thermo-mechanical modeling.

Etched inside the SOI wafer is the silicon waveguide that has the 45° mirror as shown in Figure 2-8(a). On top of the SOI wafer with Si waveguide and 45° mirror etched in are the four different interconnects designs. Figure 2-8(b) represented the solder balls and on top of it is Gallium Arsenide (GaAs) chip mounted onto the interconnects and it has the Vertical Cavity Surface Emitting Laser (VCSEL) in the middle as shown in Figure 2-9(b).



(a) (b)

Figure 2-9 Schematic representation of (a) bottom Si chip with waveguide; and (b) top GaAs chip with VCSEL

As represented in Figure 2-9(b) VCSEL is designed with 200 μm diameter emitter. A heat sink is attached to the photonic integrated circuit to deal with the thermal management of the VCSEL as shown in Figure 2-8(b).The photonic integrated circuit is built for free space coupling, the emission that comes from the silicon waveguide is coupled into an optical fiber as shown in the Figure 2-8(a).

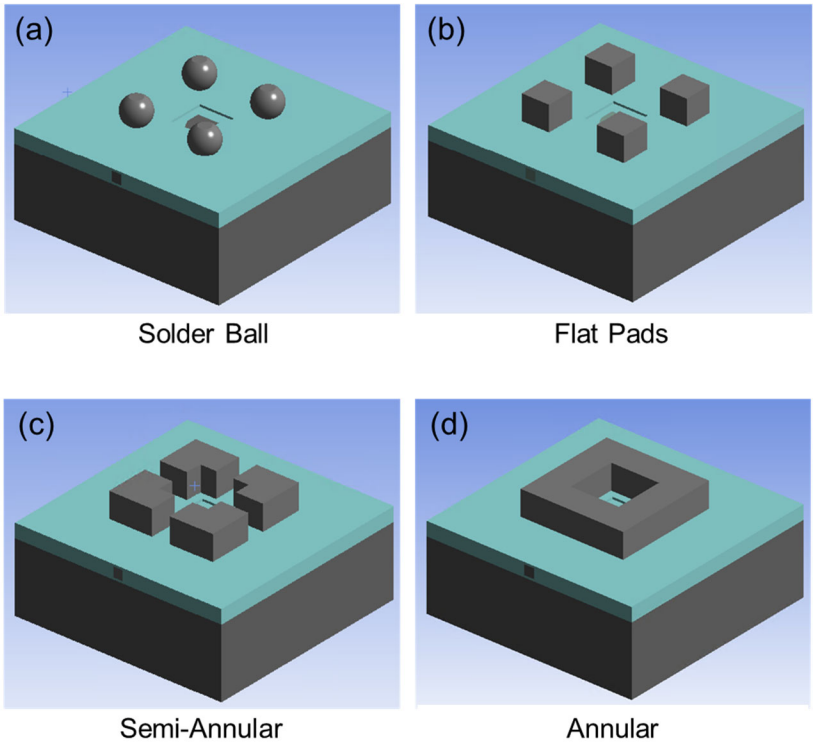


Figure 2-10 3D models of interconnect designs in photonic integrated circuit (a) solder ball; (b) flat pads; (c) semi-annular; and (d) annular deigns.

Figure 2-10 shows the four different interconnect designs. Figure 2-10(a) is the solder balls that has been increasingly becoming popular for CMOS technology. Figure 2-10(b) is the flat pad design when there is no means of depositing solder balls, standard

photolithography patterns, indium deposition and lift off processes can be implemented to deposit flat pads for applications like silicon photonics.

Figure 2-10(c) and (d) represents semi-annular and annular designs, respectively. Annular design has been in practice but can accommodate only a single interconnect design with a single input and single output connection to the device. The present study proposes the semi annular design to take the benefit of large contact area of the annular design and along with having multiple input output connections for the same component.

Depending on the device requirements, all the other models have four input output connections, but annular just has one. Depending on the application, if there is only one input output connection needed for that component then the switch on and switch off annular would be the choice.

2.5 Thermal Analysis of Interconnect Models

All the four different interconnect designs are subjected to progressively increasing heat fluxes that translate into different device powers. Figure 2-11 represents 300 mW of power being given in the 200 μm diameter area. These are high powered lasers, higher thermal distribution is expected depending on the wall-plug efficiency of the laser source. The peak temperature was observed at the laser emission source, understandably, and there are hotspots on the upper surface of the interconnects as represented in Figure 2-11.

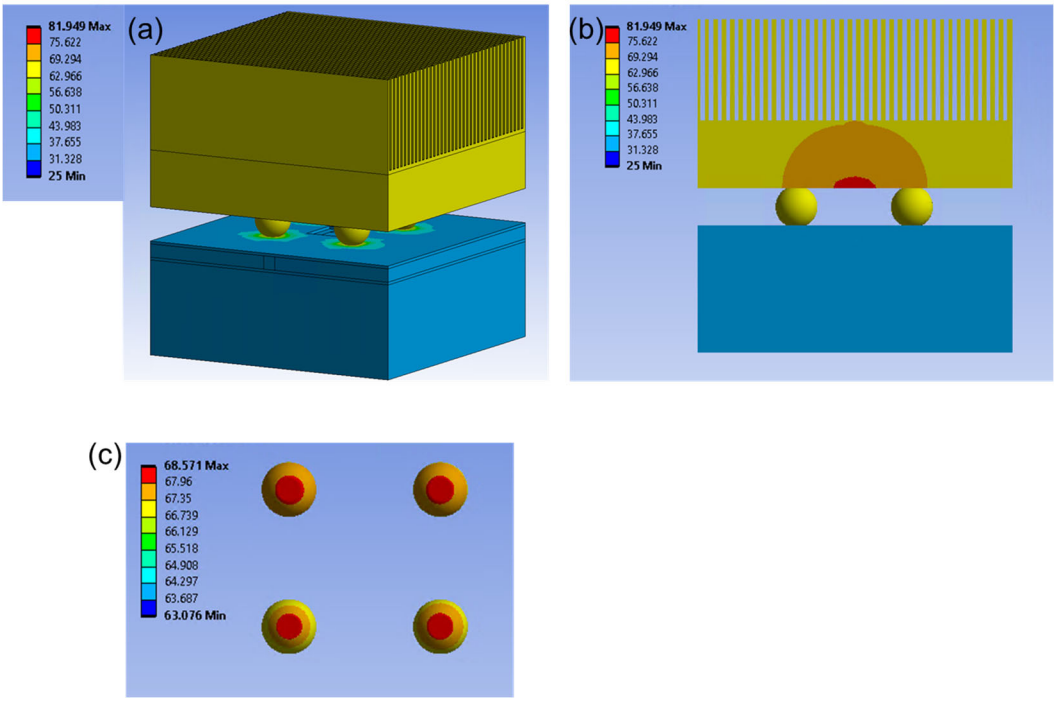


Figure 2-11 Simulated thermal distribution contour of silicon photonic device with input heat power of 300 mW showing temperature at (a) complete integrated package; (b) cross-section distribution at laser emission region; and (c) at solder ball interconnect region.

From Figure 2-12, solder ball interconnect design has the highest peak temperatures in both the device as well as the interconnects followed by the flat pad design. Semi annular follows behind flat pad design with annular interconnect design recording the lowest temperatures. The lowest temperature recorded in annular interconnect design is attributed to the highest contact area of the interconnect material with both the Si and GaAs chips. The higher the contact area, the higher the heat dissipation and absorption from the gallium arsenide towards the silicon wafer.

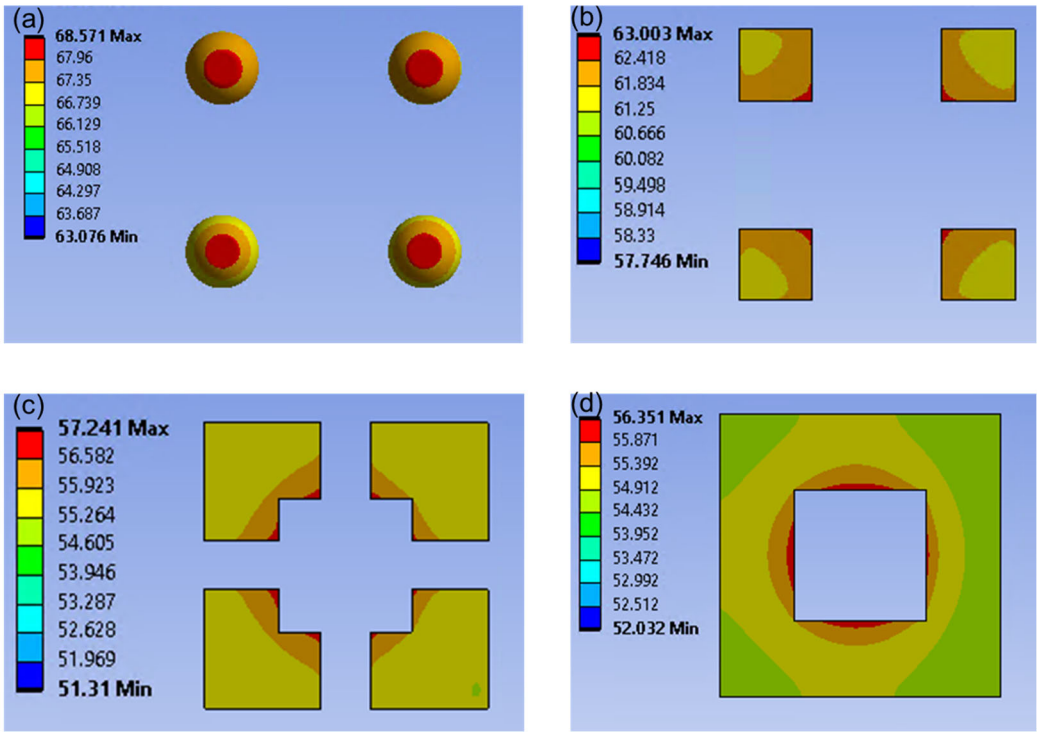


Figure 2-12 Simulation results of thermal distribution at interconnects for (a) solder ball; (b) flat pads; (c) semi-annular; and (d) annular models

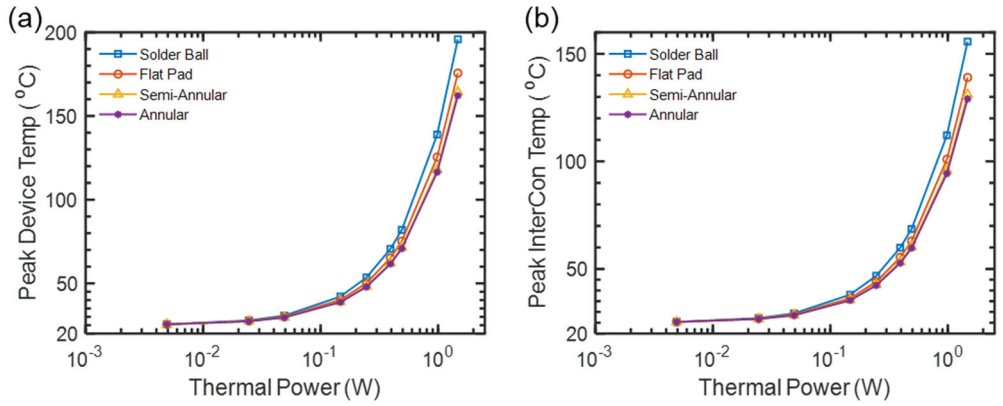


Figure 2-13 Peak temperature at (a) silicon photonics packaged device; and (b) interconnects between Si chip and GaAs chip for various thermal powers.

The graph Figure 2-13(a) represents the peak temperature recorded in the package for varying thermal powers attributed to the laser emission. The graph Figure 2-13(b) represents the peak temperature recorded at the interconnects for varying thermal powers attributed to the laser emission. Both, the device peak temperature as well as the interconnect peak temperature follow the same pattern.

At lower thermal powers, all the four designs have almost the same device and interconnect peak temperatures. As the thermal power starts scaling higher, the peak temperature increases exponentially.

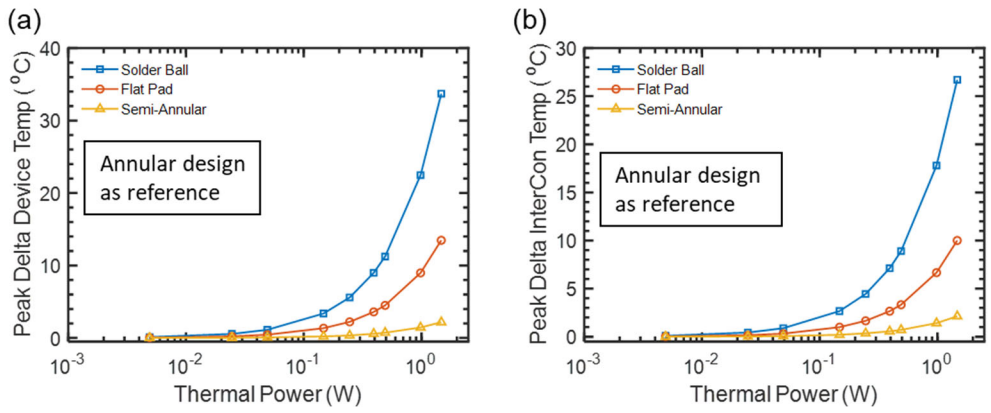


Figure 2-14 Peak delta temperature with reference to annular interconnect deisgn at (a) silicon photonics packaged device; and (b) interconnects between Si chip and GaAs chip for various thermal powers.

Annular interconnect records the lowest temperature among all the four interconnect designs represented in the study. Hence annular interconnect is taken as the baseline and the difference in device peak temperature and interconnect peak temperature between the annular interconnect model and the other three models is evaluated in the delta charts. Figure 2-14(a) and (b) the semi annular interconnect design has almost negligible or very less delta compared to annual interconnect design. The next design that

has a little higher delta is the flat pad interconnect design and solder ball interconnect has relatively higher delta in comparison with the annular interposer in terms of peak temperature. The graphs clearly show the variation of peak temperatures among all the four interconnect designs proposed.

From thermal perspective, semi annular can be considered as the optimum designed with higher input output connections as well as higher heat dissipation capability from the device.

2.6 Mechanical Analysis of Interconnect Models

Following the thermal analysis, Ansys Static Structural was employed to carry out mechanical analysis for all four interconnect designs. Mechanical stresses generated inside the package for under thermal cycling are evaluated. The package is subjected to thermal cycling from temperature of -25 °C to 125 °C. 5 thermal cycles are applied to this quarter symmetry model with the ramp rate of 900 seconds and dwell time of 900 seconds.

Interestingly, as represented in Figure 2-15 and Figure 2-16, annular interconnect design has the lowest amount of stresses developed due to thermal cycling followed by solder interconnect design, followed by flat pad interconnect design and semi annular interconnects has the highest stresses developed due to thermal loading.

In the mechanical analysis portion, the semi annular model, which was clear winner in the thermal section, did not fare well. One of the major reasons for it is the critical corners as shown in Figure 2-15. Because there are very sharp corners in the semi annular design, there are minute areas at the corner that accumulate the highest stresses. One recommendation that can be made in this case is to round the edges and avoid sharp corners to decrease the stress concentration in the semi annular interconnect model.

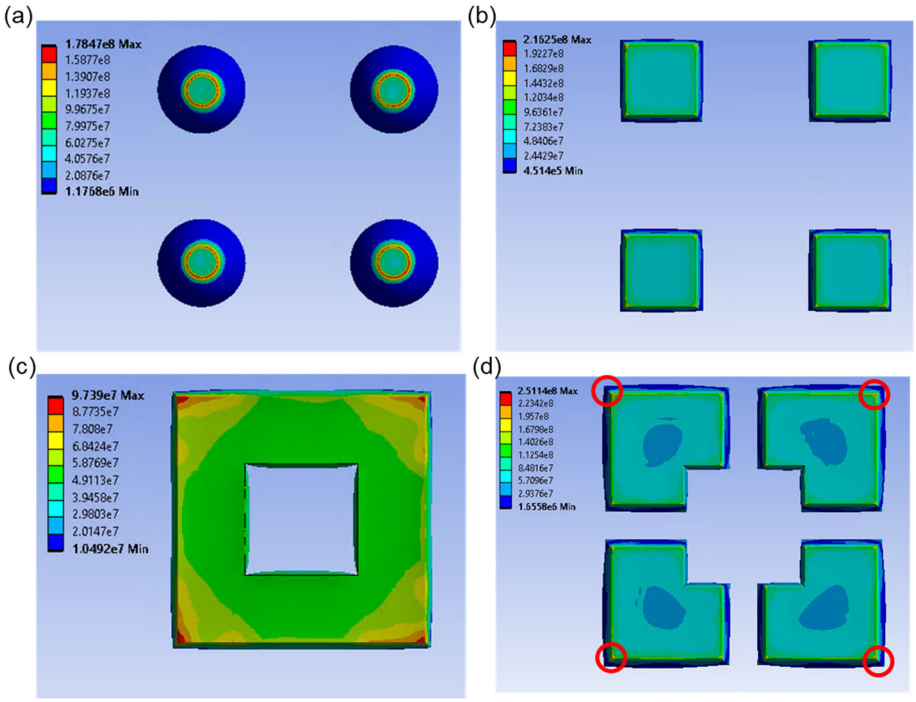


Figure 2-15 Simulation results of mechanical stress at interconnects for (a) solder ball; (b) flat pads; (c) semi-annular; and (d) annular models

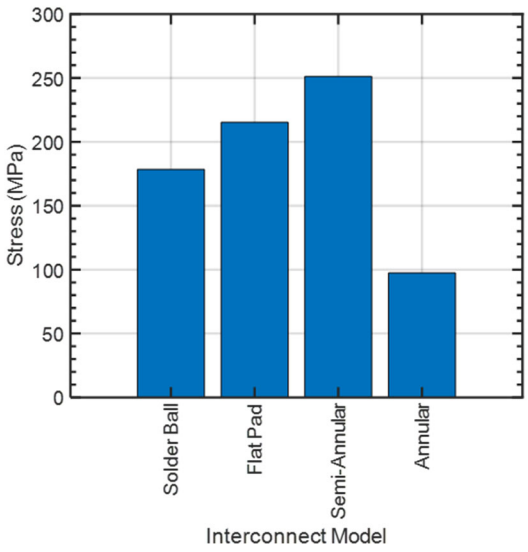
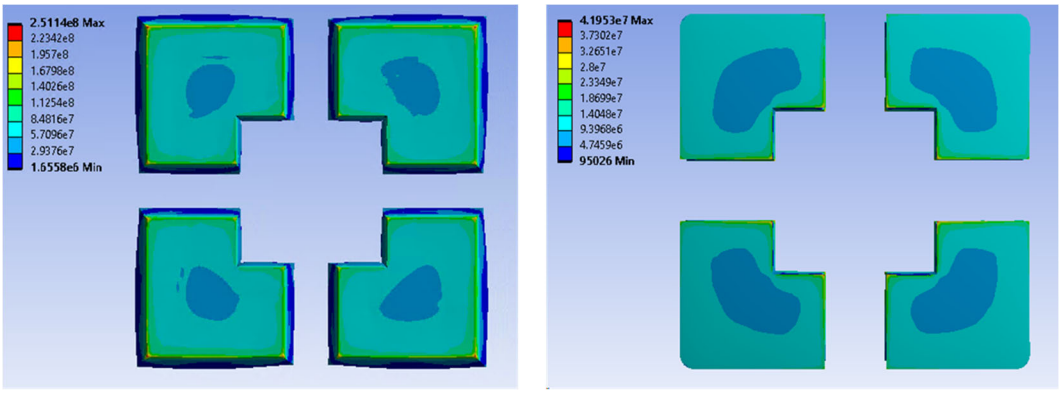


Figure 2-16 Mechanical stress at four interconnects designs simulated using Ansys Static Structural III-V/Si packaged is subjected to thermal cycle.

2.7 Rounded Corner Interconnect Model

As it was observed that the critical corners in the semi annular interconnect model are the main culprits for the higher stresses, semi annular model is modified to have rounded corners on the exterior to make sure the mechanical stresses are not being accumulated there.



(a) (b)

Figure 2-17 Simulation results of mechanical stress at interconnects for (a) semi-annular model; and (b) rounded corner semi-annular model.

From Figure 2-17 there is a significant difference in the stress accumulated in the semi annular interconnects when the corners have been rounded. Stress reduced by an order of magnitude due to smoothening or rounding the corners. In order to get better thermal and mechanical performance, rounded corners semi annular design is proposed as the optimum design among the four designs tested.

2.8 Electrical Analysis of Interconnect Models

The electrical simulations are carried out on COMSOL multiphysics software, whereas thermal and mechanical simulations were carried out using ANSYS Static Structural and ANSYS Steady State Thermal.

The current vs voltage relationship for various interconnects was established based on the current-voltage (I-V) characteristics plot. The solder balls have higher series resistance of almost 0.7 Ω compared to the 0.3 Ω in annular interconnect. The contact area on interconnects plays a crucial role in silicon photonic packages. Solder ball interconnects have the lowest contact area with the chips. This results in charge accumulation at the solder ball – Gallium Arsenide chip interface.

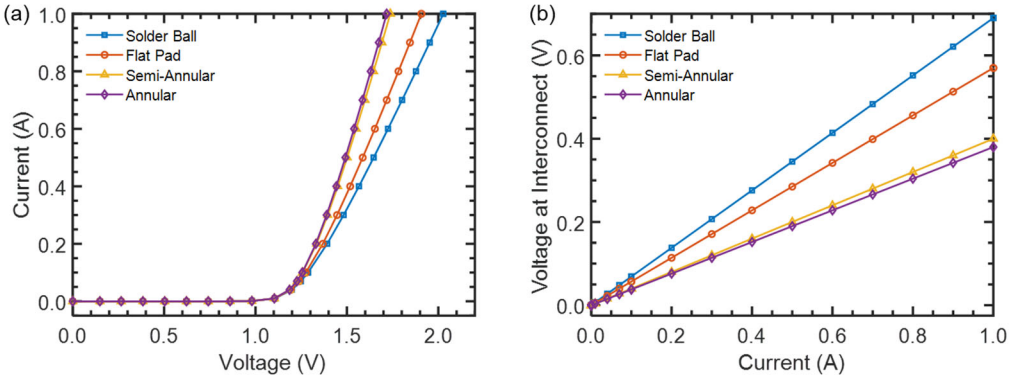


Figure 2-18 (a) Simulated I-V characteristics of III-V/Si hybrid laser device with different interconnect designs; and (b) voltage drop calculated at various interconnects for injected current.

The interconnect to chip interface is another area where hotspots are common, and they contribute to package failure. Less contact surface area means more resistance for the current. When voltage is injected into the interconnects, the current is crowded when there is higher resistance and the higher the resistance higher the current crowding happening at the interface of the interconnect and the chips. Higher resistance leads to

higher thermal hotspots. It is evident from the interconnect peak temperature graph that the solder balls record the highest interconnect temperature at the interconnect chip interface.

From Figure 2-18 the semi-annular and annular interconnects have relatively less resistance and higher current output for the voltage induced. It is especially important for devices like lasers to have higher contact area as the source voltage and current are higher for their operation.

This is in contrast to the CMOS devices, where the amount of current is relatively orders of magnitude lesser than laser devices. Solder ball interconnect design may work for CMOS devices, but for laser devices the recommendation is to go with the interconnect model that has higher contact area and lower series resistance.

2.9 Fabrication of Interconnect Models Using Flip-Chip Bonding

Flat pads, semi annular and annular interconnect designs were fabricated using Silicon wafer and Gallium Arsenide dies along with Indium solder material. Solder ball interconnect design could not be fabricated due to resource limitations. The fabrication process flow is represented in Figure 2-19

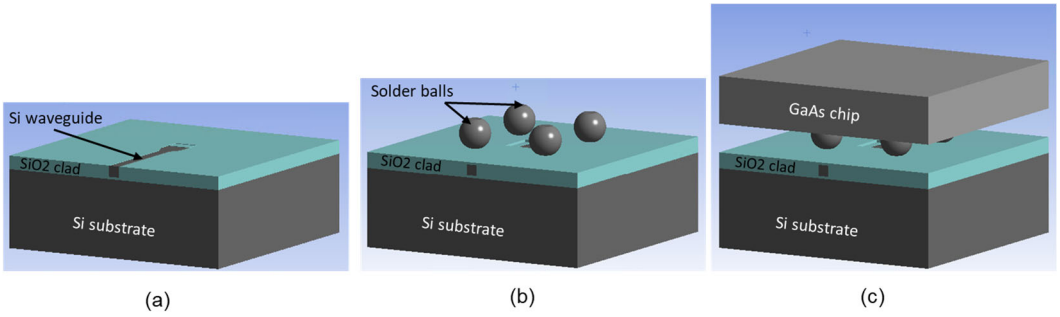


Figure 2-19 Schematic representation of the fabrication process of III-V/Si laser device (a) bottom Si Chip with waveguide; (b) deposition of interconnect pads; and (c) flip-chip bonding of Si and GaAs chips.

Standard lithography, indium deposition and liftoff processes were used to achieve these different interconnect designs as shown in Figure 2-20. The goal of this experiment is to validate the simulation results obtained for electrical with experimental results.

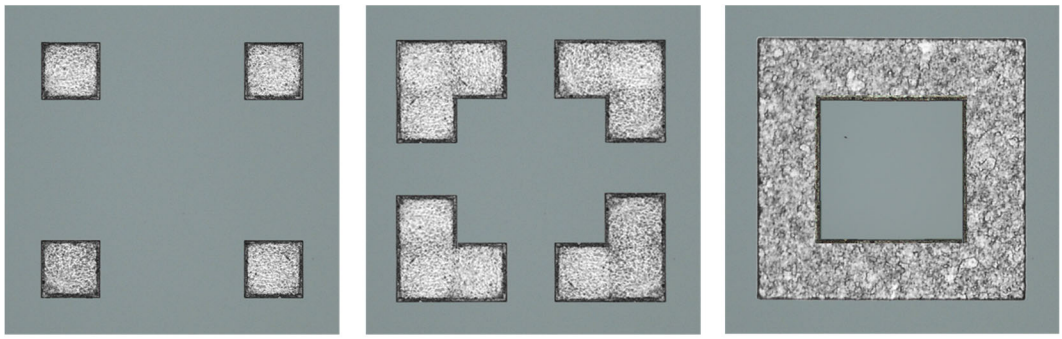


Figure 2-20 Micrograph images of fabricated indium interconnects on Si chip (a) flat pads; (b) semi-annular; and (c) annular designs

The bonding was done for all the interconnects using flip-chip bonding machine Laurier M9. Figure 2-20 shows the successful fabrication of three different interconnect design. The bonding temperature and pressure were optimized to avoid critical chip breakage failure. The temperature was scaled a little over Indium's melting temperature 170ºC until an acceptable bond is achieved. The pressure is scaled from 1 kg/cm^2 to 5 kg/cm^2 top optimize the flip-chip bonding process. At higher pressures, GaAs chip, which is relatively brittle, breaks and at lower pressures it did not have enough pressure to bond both GaAs and silicon chips. Pressure is carefully optimized to achieve reliable and successful flip-chip bond.

Though the test is not taken from standard literature, ultrasonic testing was used to assess the bond strength. The bond that withstands 2 seconds on the ultrasonicate vibrations is taken as an acceptable bond for this study. 200ºC temperature and 2 kg/cm^2

pressure for 300 seconds is identified to be the optimum temperature, time and pressure combination.

2.10 Experimental Analysis and Comparison of Models

Figure 2-21 represents the Scan Electron Microscope (SEM) images of Gallium Arsenide die, Silicon die and Indium interconnect pads. I-V characteristics of the chiplets are measured post flip-chip bonding. Figure 2-22 shows the I-V curve for simulation and experimental study of the flat pad, semi annular and annular interconnect designs. I-V characteristics are measured for the experimental chiplets post flip-chip bonding. The experimental results are in close agreement with the simulation results for electrical I-V characteristics. In both in simulation and experiment results, flat pads show high series resistance and higher voltage drop for given current. This triggers a potential device failure at the interconnect-GaAs interface.

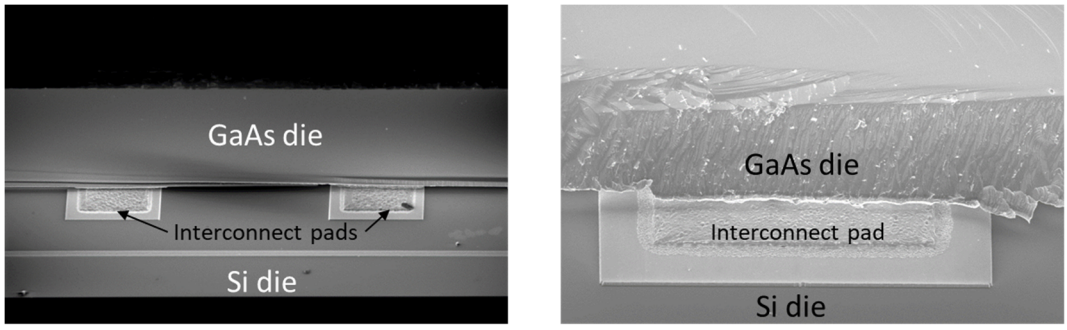


Figure 2-21 Cross-section scan electron microscope (SEM) images of flip-chip bonded GaAs-Si chip with flat pad interconnects

The device failure is much more prevalent in the flat pad interconnect design, which has a lower contact area with the chips. Solder Balls are good for low current injection applications. For high current injection applications, contact area plays a crucial role. Semi annular design is proved to be electrically better as it provides large contact area, decreasing charge accumulation and lowering the electrical resistance.

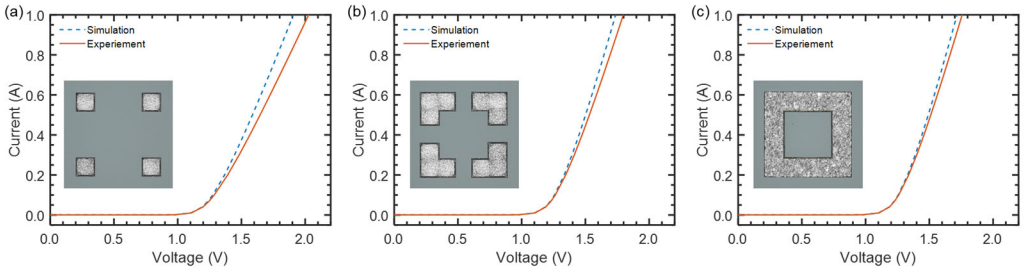


Figure 2-22 Measured and simulated I-V characteristics of GaAs-Si flip-chip bonded package with (a) flat pads; (b) semi-annular; and (c) annular interconnect designs.

2.11 Conclusion

In conclusion, four interconnect designs, solder balls, flat pads semi annular and annular designs were studied for thermal and mechanical design of photonic integrated circuit. Solder balls are good for low current injection applications like the CMOS, but for high current injection applications, especially the high-power photonic devices like lasers, contact area plays a crucial role. The semi annular design is proved to be electrically better as it provides large contact area decreasing the charge accumulation and lowering the electrical resistance. It fares well in thermal and also mechanical design perspective if the corners are rounded.

Chapter 3

GLASS INTERPOSER PACKAGE ANALYSIS AND COMPARATIVE STUDIES

3.1 Electronic Packaging Trends

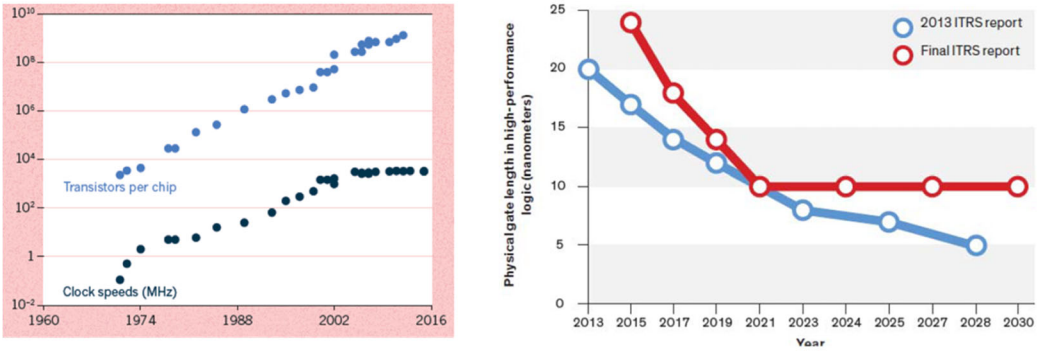
Electronic packaging refers to the back-end process where Integrated Circuits (ICs) are embedded to give rise to final products. With the advancements in semiconductor fabrication, IC feature and gate sizes have been constantly decreasing. With the IC size decreasing relative to the size of the chip, the cost per ICs has been coming down. The chips on their way to demand more power, more input output connections (I/Os) while also being compact. IC size has been the technology driver for the advancements in electronic packaging. On the other hand the market drivers for electronic packaging have been the lower cost, higher speed and performance, compactness and multi-functionality. To fulfill the technology and the market requirements, design, architectures, materials, processes, and manufacturing equipment related to the packaging industry have been changing rapidly. Wafer Level packaging (WLP), 2.5D, 3D packaging, System on Chip (SoC) and System in Pckage (SiP) are some of the industry trends enabling faster, efficient and compact electronic packages[33], [34].

3.1.1 Moore's Law

Gordon Moore laid out Moore’s Law in 1965, where it is an empirical law which states that the number of transistors will double every 18 months on the same chip real estate area. And it has been there for decades. Semiconductor ICs have contributed to shaping the modern world as we know today based on the foundation of exponential growth laid put by Moore’s Law. Semiconductor manufacturing has evolved to be a $2 trillion dollar industry with consumers getting and constantly expecting faster, comfortable and

sophisticated devices at decreasing prices every year. With the transistor size decreasing, the cost per unit area of the chip remained the same, lowering the cost of transistors and leading to lower cost per function[35]. The derivative from Moore's law says that three aspects about the semiconductor chip double every year, computer performance, CPU Clock speed because of the doubling of the third, the number of transistors per chip.

Some of the important insights Gordon Moore laid out in his 1965 article titled 'Cramming more components onto integrated circuits' include with the continuous doubling of number of components on chips every year, by 1975 the chips would have 65,000 components. He identified the major drivers for semiconductor growth to be increase in the chip area, shrinking feature sizes and improvements in circuit and device architectures. Moore predicted with the complexity of the packages increasing, the trend for doubling the transistors shifts from one year to two years, over the decades. The relatively simpler memory chips followed the trends whereas the more complex logic chips like the microprocessors were slow to catch up.



(a) (b)

Figure 3-1 (a) Plot showing number of transistors per chip and clock speeds; and (b) ITRS roadmap showing physical gate length shrinkage in transistors [36]

The semiconductor industry has been taking advantage of the empirical law and the number of transistors per chip have been increasing as shown in Figure 3-1(a), but the clock speed has been increasing until 2005, and saturated after that. Some of the complexities the semiconductor industry faced are limitations in voltage scaling, noise, leakage current and the need to innovative materials and architecture.

3.1.2 Dennard's Scaling

As In 1974, Robert H. Dennard, formulated the concept Dennard's scaling, which supports Moore's law and explains the empirical law numerically. It explains that every year the number of transistors are halved on a chip real estate by means of scaling their dimensions linearly. The key dimensions of the ICs length, width and thickness are scaled linearly by a factor of k. As the dimensions of the transistor are scaled down, the electric field across the transistor remains constant. This is achieved by simultaneously scaling down the voltage applied to the transistor. Dennard's scaling also assumes that the mobility of charge carriers (electrons or holes) within the transistor material remains constant as dimensions are scaled. This implies that the carriers move with the same efficiency even as the transistors become smaller. The capacitance of the transistor should remain constant during scaling. Capacitance is a measure of the ability of the transistor to store charge, and Dennard's scaling assumed that the capacitance would stay the same even as the device shrinks.

Dennard's scaling puts forth with the shrinkage in dimensions, smaller transistors switch faster due to reduced capacitance and smaller distances for charge carriers to travel. Since the voltage is scaled down proportionally with the transistor size, the power consumption remains roughly constant, leading to a reduction in power per transistor. With

smaller transistors, more of them can be packed into the same area, increasing the overall transistor density.

Smaller transistors meant better performance as the gate length shrunk, giving way to faster switching times and performance improvements. Even with the change in the size and number of components on a specific chip real estate, the power density remained the same without scaling. This lead to improvement in computational capabilities without increasing power consumption and thermal dissipation.

And that also explains why it is difficult to scale these because the thermal and dissipation that heat dissipation in these is becoming higher with that power.

3.1.3 Dark Silicon

Then transistor saturation came in where the number of transistors multiply was still in place. But all of these transistors could not be used all at once. There could be more number of transistors, but they had to be used alternatively, making some of the silicon or transistors dark for extended periods of time, and it gave way to ‘dark silicon’. The term was coined so because of this one, the clock speeds could not be scaled above from 2005 and that's why industry is looking for other solutions.

Dark silicon was a direct consequence of the decline of Moore’s law and Dennard’s scaling. The number of transistors on a chip increased, but the ability to power all of these transistors simultaneously without exceeding power constraints became a significant challenge. Even though the number of transistors continued to grow, the power budget available to a chip remained relatively constant.

All the transistors could not be powered all at once without producing excessive heat making the inactive portions dark silicon, switched off to manage power consumption and reduce thermal hotspots. Alternative techniques to gate the power were explored for

chip in heterogeneous architecture where different parts of the chip have varying levels of power and performance characteristics. These approaches help manage power consumption by activating or deactivating specific sections of the chip based on workload demands.

With the introduction of dark silicon, the importance of energy efficiency took a backseat in the modern chip design strategies. As the customary strategies of improving performance such as clock speeds enhancement and performance improvement weren't being fruitful anymore, there is a paradigm shift towards optimizing power usage and exploring alternative architectures such as More Moore approach and More than Moore approach to make the most effective use of available resources.

3.1.4 More Moore and More than Moore approach

More Moore (MM) and More than Moore (MtM) approaches are improvements to Moore's law to further semiconductor manufacturing with improved clock speeds and performance. The approaches aim at furthering semiconductor advancements by taking care of the traditional scaling challenges and limitations.

When the chips of same functionalities are stacked together, it gives way to More Moore approach. When chips of different functionalities are stacked together in 3D fashion, it gives way to More than Moore approach and heterogenous integration.

The More than Moore approach understands that a mere scaling down of transistors is no longer improving the necessary features in a package configuration or addressing the clock speed saturating. So MtM approach focuses on diversifying functionalities along with improving functionality density of the chip real estate. Coming together of chiplet with different functionalities, to form system in package and system on chip configuration is called heterogenous integration.

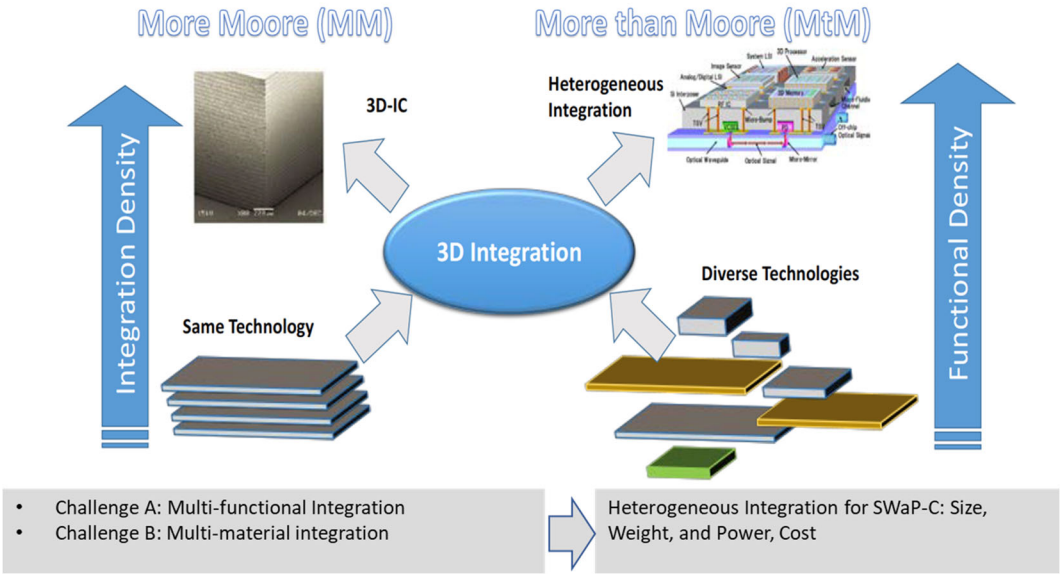


Figure 3-2 Schematic representation of More Moore (MM) and More than Moore (MtM) approaches [36]

3.2 Heterogenous Integration

IEEE defines Heterogeneous Integration to be “the integration of separately manufactured components into a higher-level assembly that, in the aggregate, provides enhanced functionality and improved operating characteristics”.

Heterogenous integration is an umbrella term that encompasses a broad spectrum of technological element, from transistors, transistor fabrication, gate length, node manufacturing to testing and packing transistors. Heterogenous integrations does not merely represent the continuation of Moore’s law but it aims at increasing the functionality density of the chip real estate[37]. This is achieved by stacking chips with different functionalities on top of each other in 3D fashion. Moore laws takes care of its approach where performance is increased by same function and increasing the number of components of the same function in contrast to heterogeneous integration[38].

Historically the functionality improvements were largely confined to chip level, where with the introduction of heterogenous integration, they are being scaled to package level. With the limitations posed by 2D integration in increasing the integration density, more interest is directed towards 3D chip and package architectures. 3D stacking is successfully demonstrated in memory chips but has it's limitations in the form of thermal management and hotspots in processor chips regime. Efforts are being made to expand 3D integration architecture to process chips.

3.3 2.5D and 3D Integration

Limitations in functionality and performance improvements gave way to two different chip architectures namely 2.5D and 3D integration. In 2.5D integration there is an interposer or a piece of interposer or bridge. It can be organic silicon or, as in the case of the current project, the glass interposer.

In the Figure 3-3 the package hosts a silicon interposer, so when there are no active chips on both sides of the interposer, when the chips are side by side, but to increase the signal and extend the signal to wider pitch if interposer is taken interposers help is taken then it is called 2.5D integration.

2.5D integration enables higher density of interconnects because there are no wire bonds. The distance between the source and the receiver has been cut down rapidly because of the use of through package vias and redistribution layers. The signal transmission can be faster using 2.5D and 3D integration, there can be active and passive interposers where in passive interposers the only job of the interposer is to carry the signal. But in active case there can be different smaller devices embedded inside it[10].

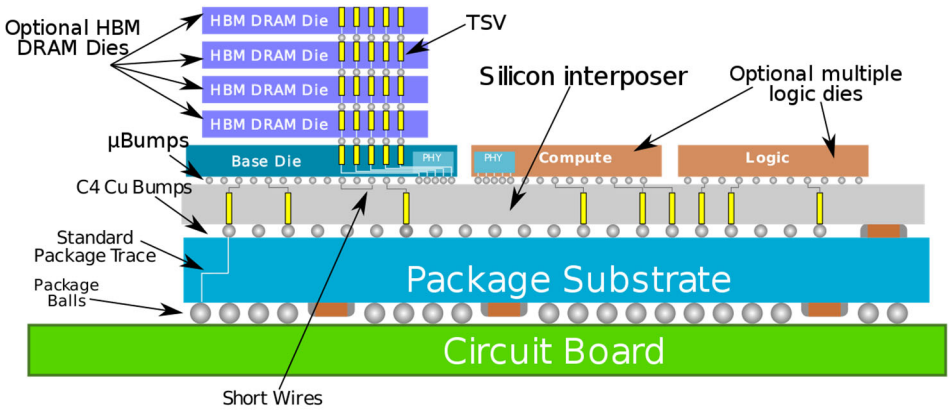


Figure 3-3 Schematic of Silicon Interposer based 2.5D Integration showing various functional chiplets integrated in a single chip[39]

The interposer also provides mechanical strength and has several functional components in it. Especially when there are differences in the Coefficient of thermal expansion (CTE) between the die and the PCB or any two layers being attached and facilitated by the interposer, it absorbs large amount of stresses induced by external factors such as thermal cycling or thermal loading.

The positives of 2.5D integration come up to be reduced size because the signal transmission distances are shorter. There is no wire bonding involved here. The speeds are higher, the power usage is lower, the heterogeneous integration can be used with interposers in place. Different technology nodes can be combined into a single component. In some cases there is a CTE match between Die and interposer[40].

In the case of silicon interposer, the dye material and the interposer material are the same, so the amount of stresses can be reduced. But on the flip side, it is a complex integration scheme. It needs several improvements in the thermal management area. There are reliability issues concerning the solder interconnects as well as through package via speed through silicon vias, through organic vias or through glass vias, which is the

analysis topic for this project[41]. The cost of interposers, especially silicon interposers can add significantly to the overall cost of the package[42].

3D integration is when there are active chips on either side of the interposer and the chips are stacked on top of each other. It can be same configuration of chips or different configurations of chips being stacked on top of each other in vertical integration. 3D integration packages can also take advantage of active interposer in the same way 2.5D integration does[43].

Some of the advantages of 3D integration over 2.5D integration include reduced size compared to 2.5D packages. It is estimated that the 3D are 35% smaller and compact in comparison to 2.5D packages. Further 3D integrated packages give way to even smaller and compact normal multi chip modules. They have increased functional density because on the same real estate we have higher number of chips.

They also have shorter wiring leads because the major wiring or the signal carriers are routed by means of the through package via and not the wire bonding interconnects. The power consumption can be 50% less and the capacitance is reduced. The bandwidth in 3D packages can be scaled up to 8 times, and especially if the silicon interposer is being used, it can go to finer pitches[44]. That's where organic interposers are lacked. But still, studies are underway to improve in that area as well. The major issue in the 3D integration is thermal performance, because with all the chips on it to work the heat dissipation methodology must be improved drastically. 3D packages demand highly efficient heat sinks and thermal vias.

They need critical interconnect routing to avoid hotspots. The interconnects through package are filled with copper. Through package vias are used for both electrical as well as thermal purposes to dissipate the heat. Through silicon, we are generated stress

between the interposer material and cocoa material can also be a problem for the reliability, the design and integration course are higher in this 3D integration as well.

3.4 Organic, Silicon and Glass Interposer Technologies

Organic interposers have poor mechanical strength. The organic interposers fall short in their mechanical properties, such as strength and bulk modulus, Young's modulus. There are challenges in fabricating finer pitches, which is under research. Organic interposers also have higher CTE mismatch with silicon die[45]. All these contribute towards the reliability failures of organic interposers.

Silicon interposers may be good for finer pitches, but they have higher cost because their wafer size is limited. They do not come in large panel processes and the electrical losses for high performance application is much higher in silicon interposer when compared to glass and organic interposer[46][47].

Glass interposers, though they have their own share of problems like still struggling with finer pitches, but have better electrical properties, low loss and low cost because they can mass produced in panel fashion and glass interposer panel size can be as high as eight times compared to the silicon interposer[48].

High thermal resistance, optical transmission and high chemical durability all contribute to glass interposers merit and glass interposers have just emerged as the new interposer technology and a lot of work is being done in this area[49][50]. The present study is about a glass interposer package design where the glass interposer comes in the middle. Here is the glass interposer has chips on either side right and left on in the middle there is there are two chips on the top and the bottom and these chips[51].

3.5 Glass Interposer Modelling and Simulation

In the glass interposer package as shown in Figure 3-4, the response of copper via and glass interposer interface to thermal cycling is one of the major focus areas of the present study. The Mechanical properties of the components and materials used in the glass interposer package model are reported in Table 3-1.

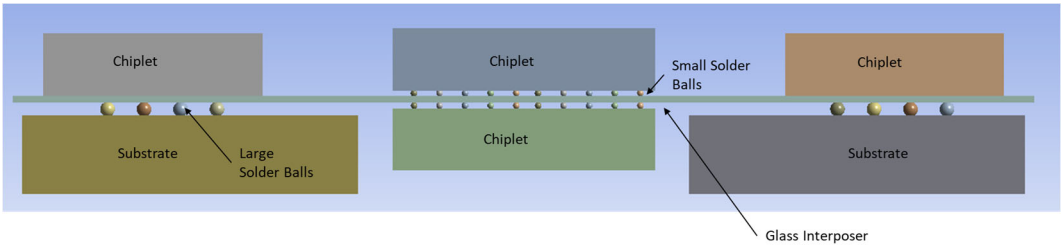


Figure 3-4 Schematic representation of glass interposer package design

Table 3-1 Mechanical properties of the components and materials used in the glass interposer package model[52]

Component	Material	Young Modulus (GPa)	Poisson's ratio	CTE ppm/K
Glass interposer	Borosilicate Glass	64	0.2	3.3
Via	Electroplated Copper	70	0.34	18
Solder Balls	SAC 305	Temperature dependent	0.35	Temperature dependent
Chips - Large	Silicon	130	0.28	2.8
BT Substrate	Glass/Epoxy resin	15.2	0.195	15
PCB	FR4	22	0.28	18

3.5.1 Modelling and Simulation

The package has quarter symmetry, 1/4 symmetric model has been taken for analysis to save on computational power. Towards the middle of the package, the glass interposer has chiplets attached to the top and bottom. To facilitate communication

between the chiplets on either side and also route the connections to other components of the package, circular holes called through glass vias or simply vias are drilled into the glass interposer as shown in Figure 3-5. The vias are filled with copper that carry the electrical signals from one part of the package configuration to the other.

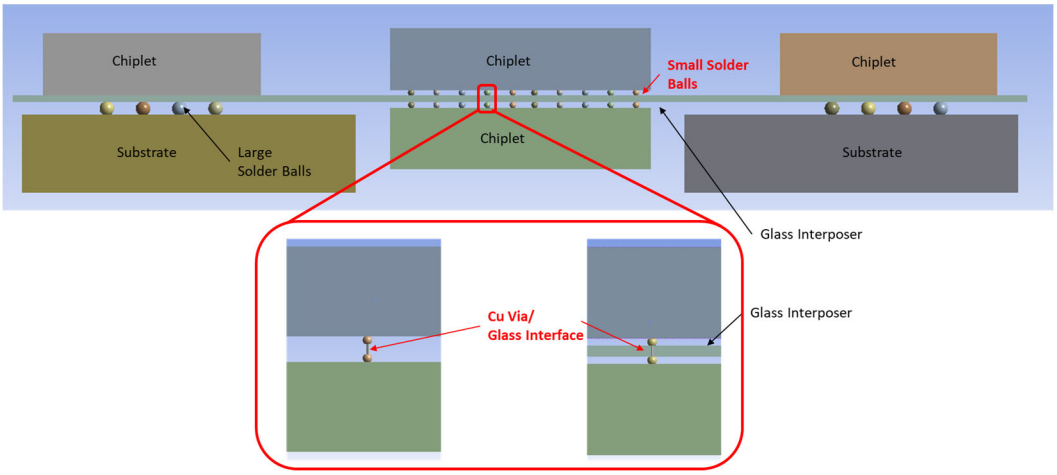


Figure 3-5 Schematic representation of the glass interposer package with zoom-in view of Cu Via and small solder balls in the inset

The glass interposer package was subjected to thermal cycling from temperature of -25 °C to 125 °C according to JEDEC Standard. 5 thermal cycles were applied to this quarter symmetry model with the ramp rate of 900 seconds and dwell time of 900 seconds.

3.5.2 Stress at Cu Via/Glass Interposer Interface

The Copper via and glass interposer interface response to thermal cycling is one of the major focus areas in this study. Foremost player in the stresses is the CTE mismatch between the copper and borosilicate glass. Copper has a CTE of 17.3 ppm/°C, whereas

glass used in this study has a CTE of 3.3 ppm/°C. The huge mismatch in CTEs has detrimental effect on the stress incurred at the Copper-Glass interface.

Glass has a tailorable CTE. The glass chosen for the study is borosilicate glass which has a CTE of 3.3 ppm/°C, which is in close match with silicon chiplet on the top. The CTE match, reduces the stress between silicon chiplet and glass.

Because the comparative CTE is quite low for glass and it's quite high for the copper that is filled inside the glass when there is high temperature, copper tries to expand more and glasses resisting it. With lower temperature when it comes to the -25 degrees, the copper is contracting more and glasses again restricting the motion of copper as shown in Figure 3-6. There are critical corners at the top where the stressors are accumulated because of the CTE mismatch[53].

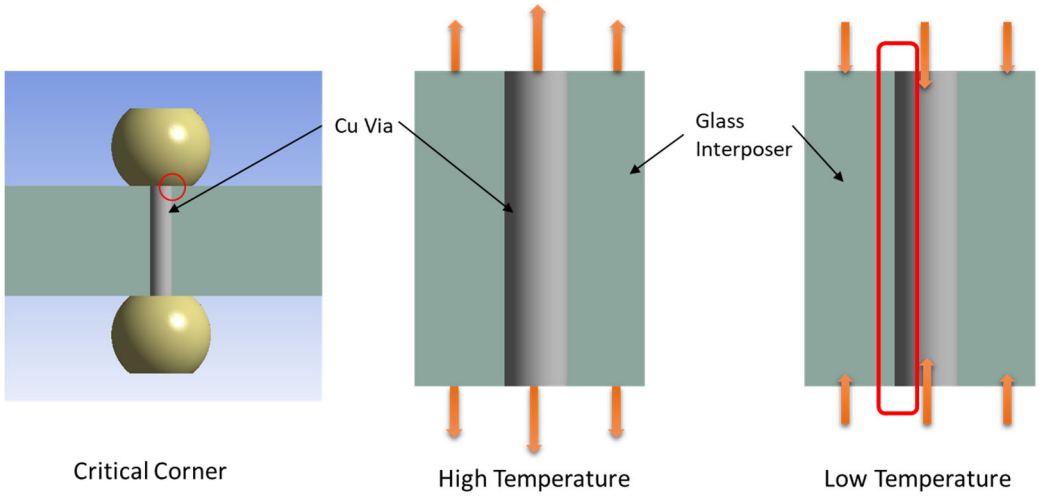
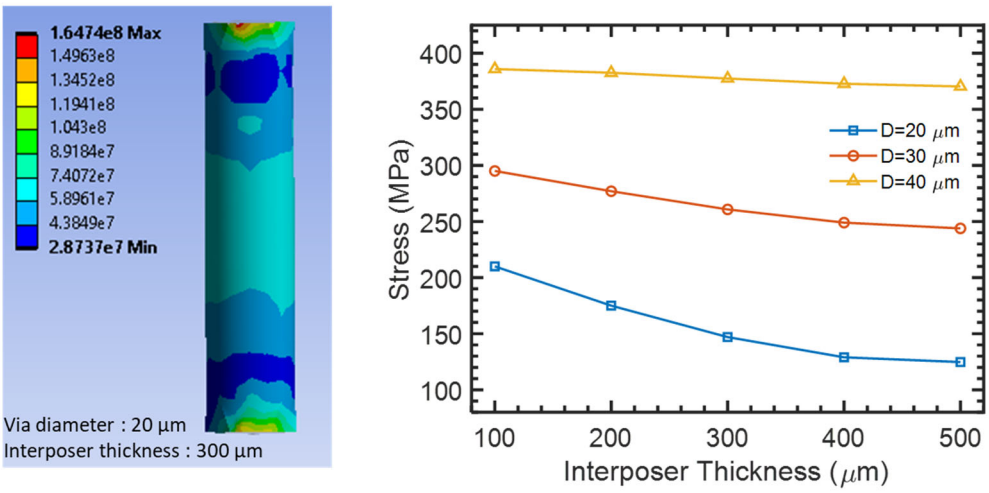


Figure 3-6 Schematic representation of Cu Via/Glass Interface showing expansion and compression mismatch under high and low temperature impact.

The interposer thickness is scaled from 100 µm to 500 µm with 100 µm increments. 100 µm is thinnest glass interposer, but it is being studied for miniaturization of the package design. The commercial glass interposer thicknesses range from 100 µm to 500 µm. The

diameters of the via are taken as 20 µm, 30 µm and 40 µm. The via diameters are proven to be possible in fabrication. The analysis was done for combination of five thicknesses and three diameters as shown in Figure 3-7(b).



(a) (b)

Figure 3-7 Simulated results for stress at Cu Via/Glass interface (a) temperature contour for 20 µm via diameter and 300 µm interposer thickness; and (b) for all via diameter and interposer thicknesses

From Figure 3-7(b) the stress at the Cu Via/Glass interface was relatively less affected by the thickness of the interposer. The change in stress at the interface was relatively larger at smaller thicknesses and gradually saturated as the thickness increased. From Figure 3-8 stress at the glass-copper interface increased linearly with increase in the via diameter from 20 µm to 40 µm.

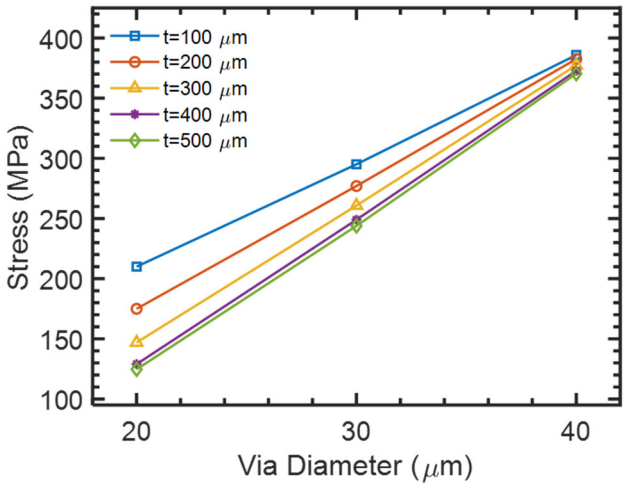


Figure 3-8 Simulated results of stress developed at Cu Via/Glass Interposer interface for various via diameters.

3.5.3 Stress at Small Solder Ball

The stress in the solder was relatively less affected by the thickness of the interposer. Stress decreased gradually with thickness and almost saturated at higher thicknesses. For each thickness, the stress in the solder ball increased linearly with increase in diameter. From the given data 20μm diameter and 300μm thickness is the optimum via diameter/interposer thickness combination for low stresses in interposer solder balls.

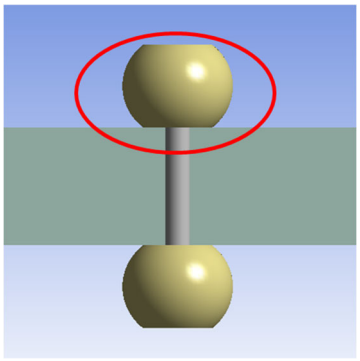


Figure 3-9 Schematic showing the small solder ball and glass interposer interface.

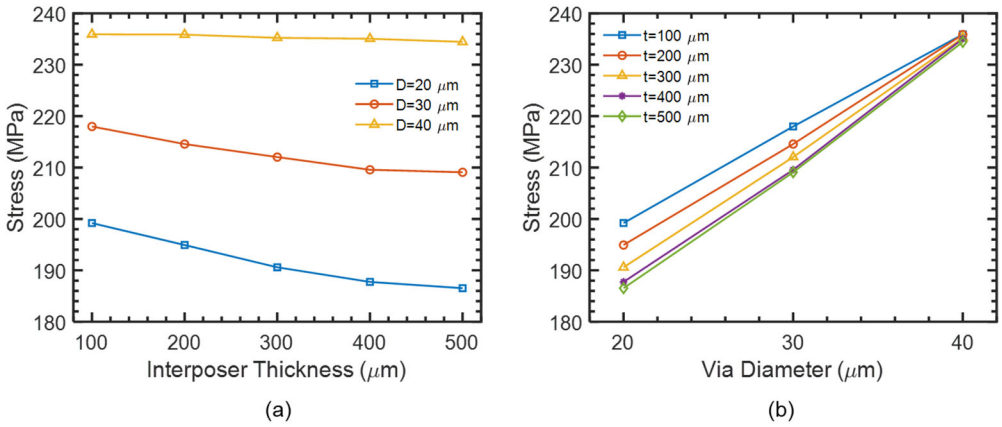


Figure 3-10 Simulated results of stress at small solder ball and glass interposer interface.

3.5.4 Stress at Large Solder Ball and Chiplet Interface

The thickness of the interposer had minimal affect on the stress in the large solder ball. For every thickness, the stress at the interface of chiplet and interposer with no interconnects is higher than the chiplet and interposer interface with solder interconnects as shown in Figure 3-13(b). This is due to solder interconnects absorb the stresses arising from CTE mismatch between the glass interposer and silicon chiplet. The stress trend in solder ball based chiplet interposer interface has lower slope compared to the no interconnect case indicating solder balls absorb most of the stress.

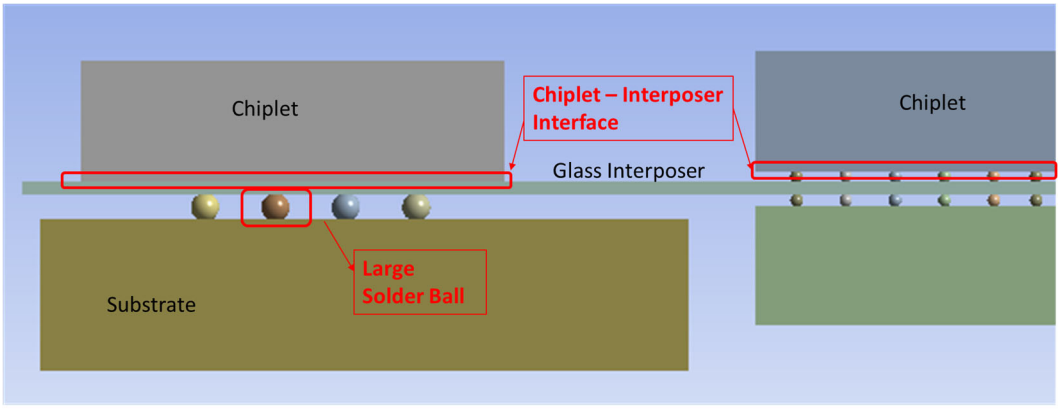


Figure 3-11 Schematic representation of glass interposer package with chiplet-interposer interface and chiplet-solder ball-interposer interface.

3.5.5 Total Deformation in Glass Interposer

And the final steady did on this one is the total deformation and the glass interposer in all three directions X, Y and Z as shown in Figure 3-12 for 100 µm thick interposer. So for different thicknesses, the total deformation in the glass interposer was taken into account and here too with the increase in the thickness of the interposer, the stresses came down almost linearly. The highest deformation being for 100 µm and the lower stresses recorded at 500 µm thickness of interposer. This can be attributed to the ticker interposer requiring higher thermal stress to deform and thus resisting the deformation for some extent.

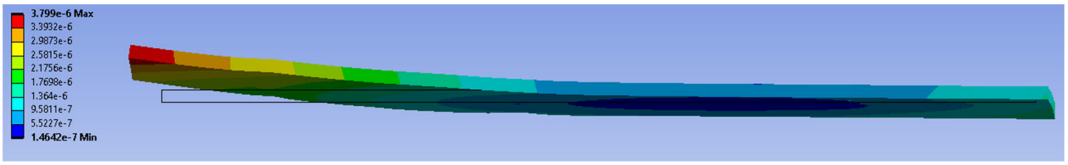


Figure 3-12 Structural deformation observed in glass interposer model of 20 µm via diameter and interposer thickness of 100 µm when subjected to thermal cycling.

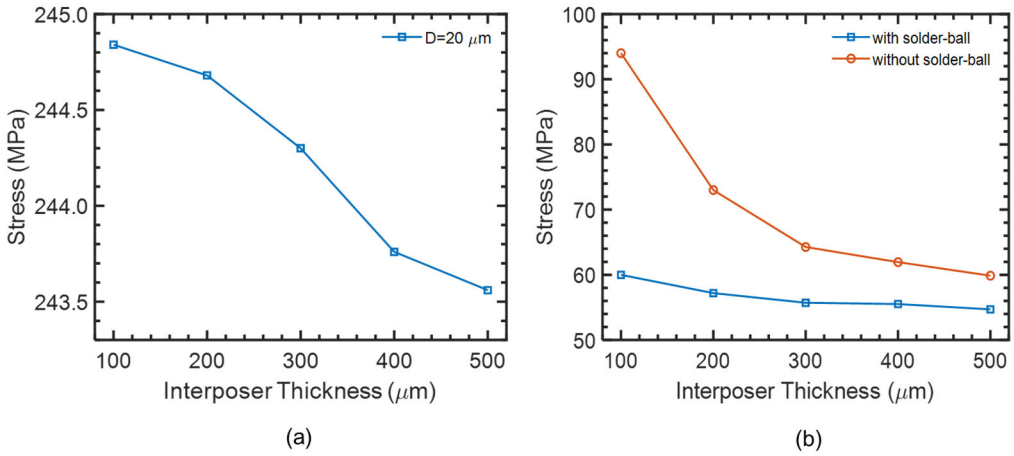


Figure 3-13 Simulated results of stress in glass interposer package at (a) large solder ball interface; and (b) chiplet-interposer interface and chiplet-solder ball-interposer interface

3.6 Conclusion

In conclusion, the stress in the solder was relatively less affected by the thickness of the interposer and the stress decrease gradually with thickness and almost saturated at higher thicknesses. To avoid the higher processing using thicker interposer, 300 μm is an ideal thickness according to the study for the thickness range of 100 μm to 500 μm. For glass interposers, the thickness of the interposer had minimal effect on the stress on the substrate. Large solder ball did not take a lot of stress from the thickness difference from the interposer above it. The deformation in the glass interposer decreased almost linearly with increase in the thickness.

The stress at solder balls and copper/SiO_2 interface decreases with increase in interposer thickness till 300 μm. Beyond that it saturates. Optimum thickness for glass interposer is 300 μm with 20 μm copper via diameter for the combination of glass interposer thicknesses and through package via diameters considered for the study.

Chapter 4

SINGLE PHASE IMMERSION COOLING OF TWO SOCKET SHADOW CORE SERVER

In a typical data center, it is reported that among all the electricity supplied to the data center 52% goes towards the IT gear, 38% is consumed by the cooling system employed and the rest is taken up by miscellaneous components [54]. Cooling system is paramount to the proper functioning of the servers in the data centers as heat is the major by-product produced by the IT components. The most common and industry dominated cooling system is based on air cooling today[55]. With the constant increase in the processing and computing powers, data centers accounts for roughly 2% of the world's electricity consumption and is projected to increase by 15-20% of the current consumption each passing year[56]. Most of the data center today are designed to support aircooling. In an air-cooled data center, server fans will move the air from cold aisle and exhaust it to hot aisle[57]. Depending on the data center design, hot air will either be released into the environment or cooled by facility equipment such as chillers, air side economizers, evaporative cooling etc[58]–[61]. Over the course of the last two decades, a lot of research has been done to improve the overall airflow management. This includes some of the best practices such as hot or cold aisle containment, use of blanking panels, non-raised-floor data centers etc[62]. Although there is a successful track record of implementing air-cooling, inefficiencies still exist due to factors such as hot-air recirculation, cold-air bypass, over-pressurization etc. and heterogeneous deployment of server types/generations. The engineering costs arising from designing the data center air flow at room and rack level for each new server design brings down the overall cost efficiency [63]. To lower server fan power usage, airflow is modulated with a 5-10% thermal margin on all the critical components. For example, a CPU with a recommended maximum junction temperature of

100°C, it is common practice to modulate the airflow so that the CPU temperature is maintained between 90-95°C[64]. Operating at higher core temperature, noticeably for CPU and GPU ASICs, adversely affects the computing performance. It may also decrease the component lifetime [65]. With air cooling, it is becoming increasingly challenging to maintain a lower component temperature due to increasing power density [66]. In addition, this requires fans to operate at higher RPM thereby increasing the fan power and further reducing the efficiency of the data center. Immersion cooling is emerging as a superior alternative to air cooling[67]. Dielectric liquids that are electrically nonreactive to the servers are used to remove the heat away from the components. While air has approximated thermal conductivity of 0.026 W/m-K at room temperature, dielectric liquids usually have thermal conductivity in the range of 0.1 – 0.2 W/m-K[68]. The high cooling efficiency of the immersion liquids help in handling the increasing energy densities of the emerging electronics especially the data center servers [69].

4.1 Motivation

Submerging a cluster of servers inside a large tank is the customary way of employing single-phase immersion cooling. But this approach requires a complete renovation of existing air-cooled infrastructure[70]. A practical approach to convert an air-cooled data center to immersion cooled data center can be retaining the rack and server arrangements and supplying each server with immersion liquid in sled configuration – retaining horizontal position. The present study aims at characterizing the thermal performance of a 2-socket server in sled and tank configurations using CFD. In the tank configuration model, the server is immersed vertically with the coolant supply from bottom to top as in the case of a typical single-phase immersion deployments. In the sled configuration, the server orientation is retained (horizontally) and the fluid supply is

modeled as an inlet and outlet manifold connected to the same side of the server. The CFD modeling approach is aimed to determine the heat transfer behavior of the server in two configurations being looked at was done for a commercially available dielectric immersion liquid, EC 110. A detailed baseline geometry of the server was first simplified, considering only the components that are significant source of heat and/or impact the server flow characteristics. Some of the components considered for analysis include CPU, storage drives and memory modules. The performance of the server in two configurations is compared to determine the efficiency of both the server configurations while ensuring the components do not exceed their respective thermal threshold. Component temperatures are obtained by varying the coolant flow rates and dielectric temperatures.

4.2 Modelling Methodology

For the present study an open compute server with a two-socket motherboard is chosen. The mother board has a form factor of 6.5”x 20” enclosed in a chassis of dimensions 176 X 90 X 883 mm. The chassis is designed to be compatible with Open Rack v2 rack architecture. The 2OU server is compatible with Intel Xeon processors that enhance the performance of the CPUs by increasing their frequency. These highly efficient servers can handle high demanding applications requiring high-power computing. The 32 PCIe lanes can house expansion cards for memory storage. More information about the server considered for analysis can be found in reference [9]. Figure 4-1 shows the CAD model referenced from the open compute project. The highlighted components namely the heatsinks, the CPUs under the heatsinks, DIMM chips, HDD drives, PCI card, voltage regulators and corresponding smaller heatsinks and PCB hosting all the elements were included in the study. The casing around the components, metal hosting for fans and HDD drives, screws, washer, nuts, and bolts used for the assembly, that do not participate in the

heat transfer process or obstruct the flow significantly are ignored. This was done to simplify the model and reduce model complexity and mesh count.

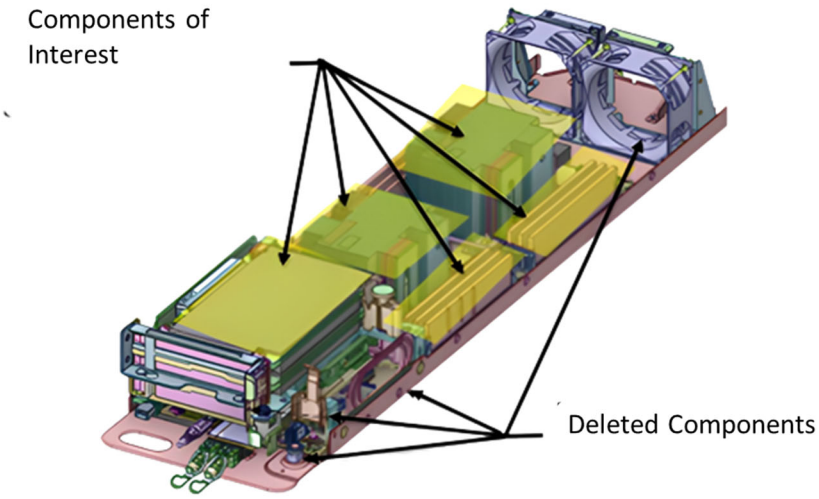


Figure 4-1 Simplified model of the two-socket server indicting components of interest and deleted components for thermal modelling requirements.

4.2.1 Modelling of Server Components

The Computational fluid dynamics-based software 6SigmaET was used to analyze the fluid flow pattern, peak temperatures and fluid velocity around various server components for both, air and immersion cooling. The simplified CAD model with components important to heat transfer study was imported into 6sigmaET software. Using the CAD model as reference, certain objects such as CPU, CPU socket, heat sink, etc. were built using 6SigmaET smart objects. Certain components such as embedded heat pipes in the heat sink were approximated. This reduced the solving time from the detail model by about sixty percent with negligible impact on the results of the key components (CPUs).

The server contains two CPUs that generates heat which is dissipated using a heatsink embedded with heat pipes, 12 DIMM chips, PCI, three HDD storage drives on a PCB. The voltage regulators corresponding to each CPU are modelled into a bulk for simplicity. As per the platform specifications from OCP [71], each CPU has a TDP of 125W. Table 4-1 outlines the material properties used for the server components in this analysis and Table 4-2 shows the heat dissipated by major components of the server.

Table 4-1 Material properties of the server components

Component	Thermal Conductivity (W/m-K)	Specific heat (J/Kg-K)	Density (kg/m3)
Heatsink	220	896	2710
PCB	0.3	880	1200
CPU	10	500	3000
Socket	0.25	1260	1010
Heat pipe	5000	1005	1.19
Other	10	500	3000

Table 4-2 Heat dissipation of server components

Component	Count	TDP (W)
CPU	2	125
DIMM	12	9
HDD	3	10
PCIe Card	1	10
Voltage regulators	2	6.5

An assumption was made that the HDDs are compatible for immersion cooling. The existing HDDs are not hermetically sealed and filled with Helium, making them incompatible to be used for immersion cooling applications.

4.2.2 Model Validation with Air-Cooled Experimental Results of the Server

The two-socket server in the study is commercially used in the air-cooled data centers. The present study aims at understanding the compatibility of the sever for immersion cooling. To validate the CAD model, the server was initially run for air cooling and the results were validated against experimental results. Figure 4-2 shows the 6sigmaET model with the two-socket server, 80 mm pull fans installed along with the air shroud to channel the pulled air into the heatsinks and all other essential components for heat transfer. Figure 4-2, also shows a single HDD. This was done to match the configuration to that of an aircooled server for which experimental test results were available. The empty space between the board and the fans is occupied by power cables (Medusa), power clip and a power distribution board to facilitate system removal. All the components lay low to the chassis and hence not considered for computational analysis.

Table 4-3 Component temperature comparison

Parameter	Experimental value	Computational result
Inlet temperature (°C)	35.2	35
Thermal Power of CPUs (W)	124.9	125
System Airflow (CFM)	30	30
CPU 0 temperature (°C)	77	76.5
CPU 1 temperature (°C)	82	83.2

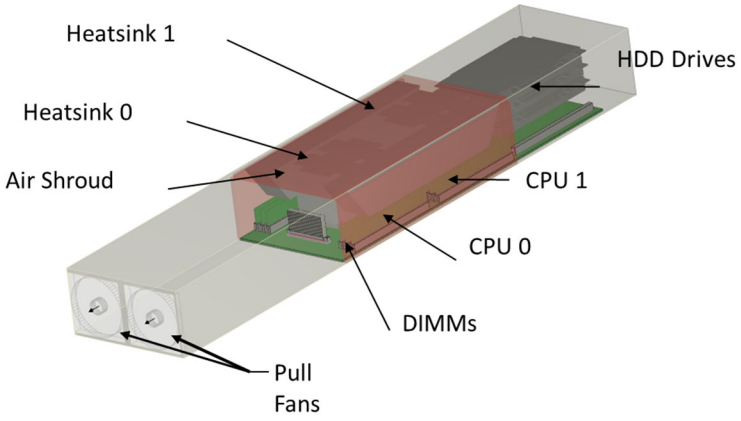


Figure 4-2 CFD model developed for air-cooled server

Table 4-3 compares the data from experimental test and CFD analysis. This was important to ensure the model is calibrated and can be used with confidence for immersion cooling study. Fans were modeled as fixed flow device as airflow from experimental measurement was available. CPU temperature under identical operating conditions was compared. CFD results show 1°C temperature lower for CPU 0 and slightly higher for CPU1. This probably could be due to modeling of VR where is modeled as lumped source. As the CPU temperature from the simulation model is in close agreement with the experimental result, the model is deemed valid.

4.2.3 Immersion Cooling modelling

For this study a commercially available immersion cooling liquid EC 110 was used to study the behavior of a traditionally air cooled two-socket server when immersed in it, for tank and sled configurations. EC 110 belongs to a class of fluids called single phase dielectric oils. The dielectric nature of the fluid limits it's electrical reactions with the server components whereas the having relatively higher melting point helps the fluid stay in liquid state without a phase change throughout the cooling loop.

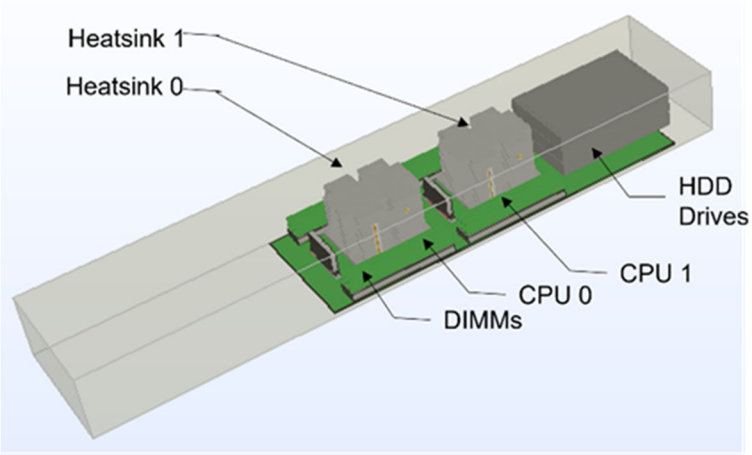


Figure 4-3 CFD model developed for immersion-cooled server.

Figure 4-3 shows the modelling modifications made in 6SigmaET to adopt the air-cooled model for immersion cooling. The fans and air shroud are eliminated. Initially the number of HDDs is kept to one but for further analysis the number is increased to three. The comparison of the models is discussed in the results section. Figure 4-4(a) and (b) illustrate the thermal properties of fluid EC 110. The temperature dependent density value of EC- 110 is taken as 839.3, 832.7, 826.1 kg/m3 at 30°, 40° and 50°C temperatures respectively. The thermal conductivity of the fluid is in the range of 135 W/m-K.

Localized mesh was defined for components of interest namely the heatsink, TIM and heat source. Mesh sensitivity analysis was performed based on CPU temperature for 3.26, 4.15, 4.4, 5.02 and 9.01 million grid cells. Increasing the grid count from 5.02 million to 9.01 million resulted in less than 0.2°C variation in CPU temperature. As a result, 5.02 million grid count was used for analysis.

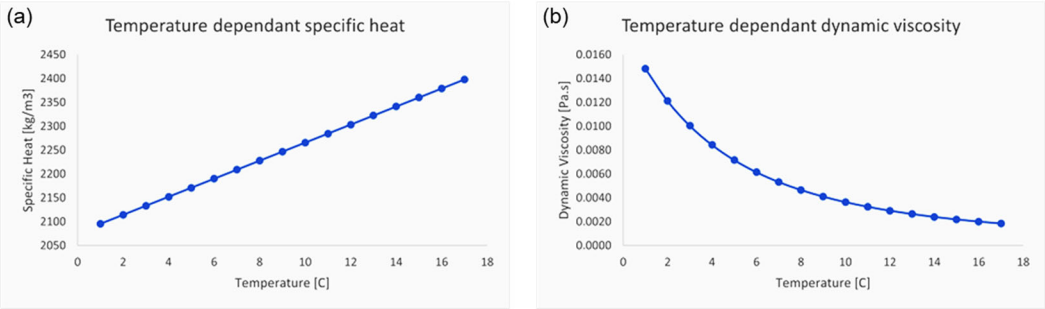


Figure 4-4 EC-110 temperature dependent (a) specific heat; and (b) viscocity

4.2.4 Traditional Tank-Based and Alternative Sled-Based Immersion Cooling

Traditionally a large tank filled with several servers placed upside-down, plays host to the immersion liquid loop where the whole of the bottom end of the server chassis area acts the entry area of the fluid[72]. Often open baths are used in which the tank is contained on all side except the top. The top side exposed to the atmospheric pressure avoids pressure build up and consequent explosions inside the tanks [63]. With high energy density, comparatively low space, and pumping power requirement, this seems to be the most economical way of cooling servers using immersion fluids.

One downside of this configuration of cooling is the total infrastructural modification it demands of the established air-cooled data centers. The data center industry is dominated by air-cooled systems for cooling. Though it regards immersion cooling as a potential alternative to satisfy the increasing trend of computational needs, the total demolition and reconfiguration of the suit with tank-based configuration can prove to be a bottle neck in adapting the immersion cooling technology.

An alternative to save the major infrastructural changes is to retain the servers in the racks as set up for air cooling and retrofitting them with necessary components to facilitate the supply of immersion liquid. There are several ways to distribute the fluid like

a data center level Cooling Distribution Unit (CDU), rack level CDU or even placing a heat exchanger inside the server making it an independent entity.

4.2.5 Modelling of Tank Configuration

For the tank configuration, a single server among a cluster of servers placed in the large tank was analyzed. As the server is placed upside down, the gravity is acting towards the bottom, the whole bottom face acts as the inlet area to the individual server and the fluid is taken out through the other end as shown in Figure 4-5.

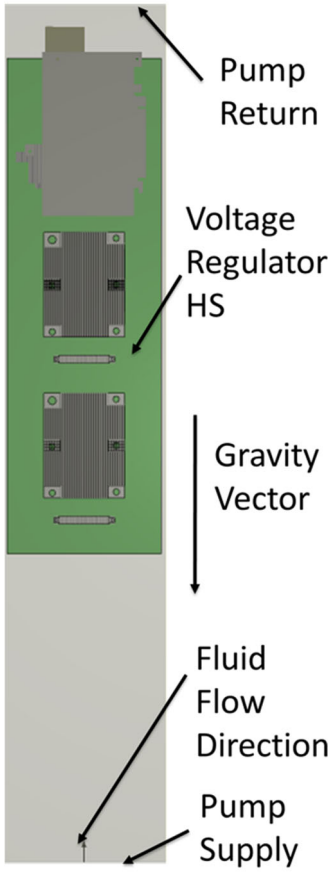


Figure 4-5 CFD model developed for tank-based server.

4.2.6 Optimization of Inlet and Outlets of Tank for Sled-Based Server Configuration

When modelling the server in sled configuration, mounted on a rack, and supplied with fluid from one side of the server, 10 mm diameter pipe openings are assumed for supply and return openings. The location of the supply and return openings affects the flow direction, flow mixing and ultimately the peak temperatures of the CPUs. Four different combinations of supply and return opening areas as shown in Table 4-4 were analyzed to optimize their location, by taking the peak temperature of CPUs in each case as the judging parameter. Supply and return are placed on the farther end face of the server. Supply and return locations on the Figure 4-6 are chosen to be the optimized locations and used for further analysis as that placement configuration results in the least peak temperature of the CPU1.

Table 4-4 Supply and return location optimization for sled configuration servers.

Supply location	Return location	Max. CPU Temp. (C)
Middle	Top left corner	64
Top left corner	Bottom right comer	65.8
Bottom right corer	Top left corner	76.1
Left side as in Figure 4-6	Right side as in Figure 4-6	60.1

To analyze the effect of flow rate and fluid inlet temperature on the heat transfer of the fluid; three cases of 1, 2, and 3 lpm and three different inlet temperatures 30°C, 40°C and 50°C were chosen. Lower flow rate makes the setup economic by saving the pumping power. Though higher temperature increases the failure rates of the components along with the pumping power. Understandably lower inlet temperatures result in lower temperatures of the server components, the recirculating fluid needs to be constantly

cooled down to the lower entry temperature. Higher inlet temperature decreases the load on the heat exchanger in the cooling loop. So, it becomes important to optimize both the fluid inlet temperature and flow rate to obtain the server component temperatures in the acceptable range.

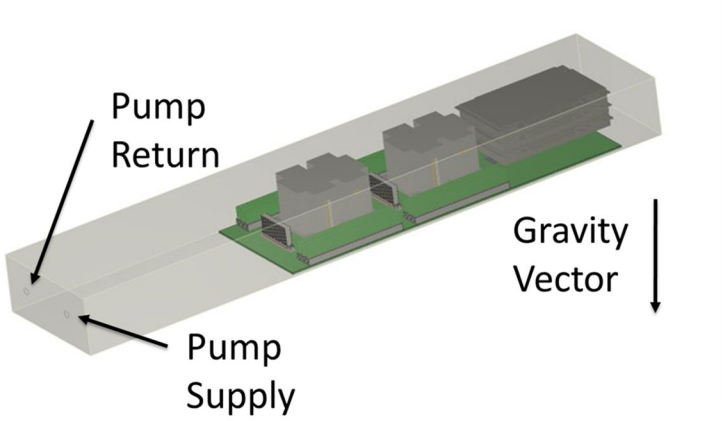


Figure 4-6 CFD mode developed for sled configuration server

4.3 Results and Discussion

From Table 4-3, the experimental results of air cooling show the peak temperature of the CPU is in the order of 80°C. With immersion cooling, even with elevated fluid inlet temperatures, the peak temperatures stay below 70°C. Higher thermal mass of the fluid compared to air, increases the Reynold's number of the fluid. Higher Reynold's number translates to higher convective heat transfer coefficient enabling the fluid to pick up more heat from the sever components.

Due to the inlet flow region being different, the immersion cooling method of cooling, allows the usage of full capacity or three HDDs with no rise in the peak temperature of the CPUs or overall fluid temperature. On the other hand, in air cooling, use of all the

three HDDs would increase system impedance, thus resulting in limited flow of air into the server and limited cooling. This would require fans to operate at higher speed increasing fan power. Figure 4-7 shows the temperature plane located at the CPU of tank configuration and sled configuration models for 30°C inlet temperature and 1 lpm flow rate. Figure 4-8 show the CPU temperature in tank-based and sled configuration respectively. Comparing the two plots, CPU temperatures for both configurations models are on close range, which proves that the sled-based configuration is equally good as tank-based configuration to convert air cooled servers to immersion cooling.

For both tank and sled configuration results in Figure 4-8, it can be seen that the with the increase in the inlet flow rate of the fluid, the peak temperature of the CPUs drop, signifying that the increase in the flow rate was able to absorb more heat from the server components. The biggest drop in temperature can be seen between the flow rates 1 lpm and 2 lpm. The change in CPU peak temperature between 2 lpm and 3 lpm is relatively lower.

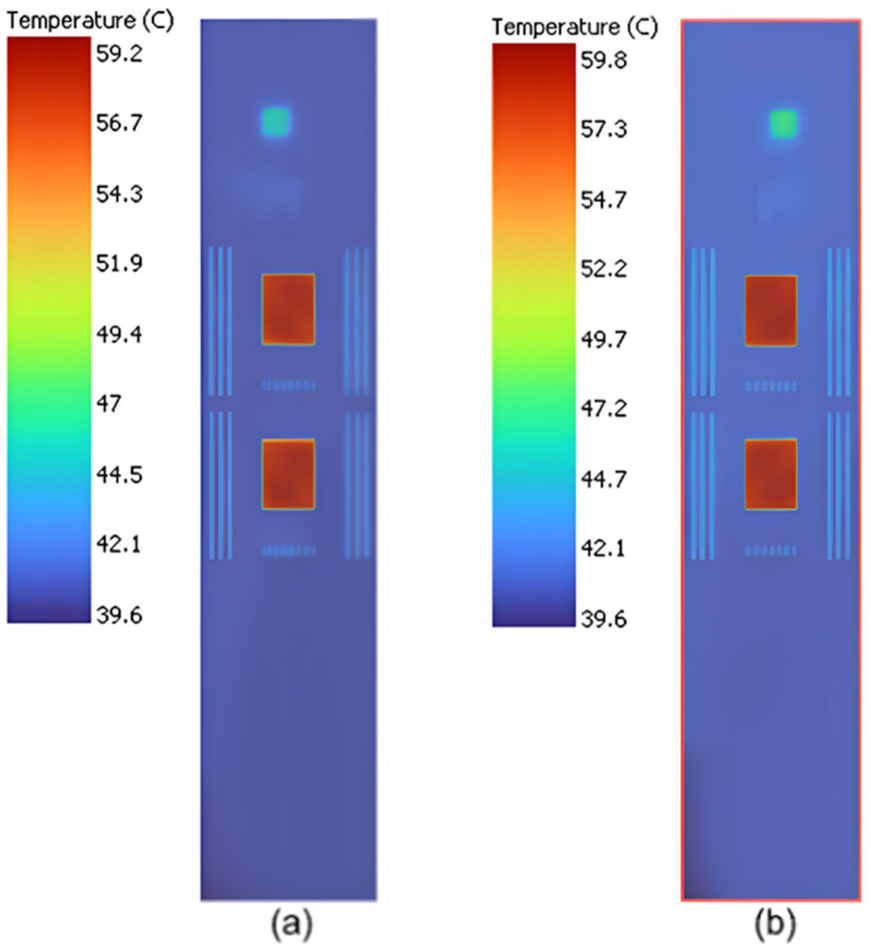


Figure 4-7 Temperature contour at the CPU of (a) tank configuration; and (B) sled configuration for 30°C inlet temperature and 1 lpm flow rate.

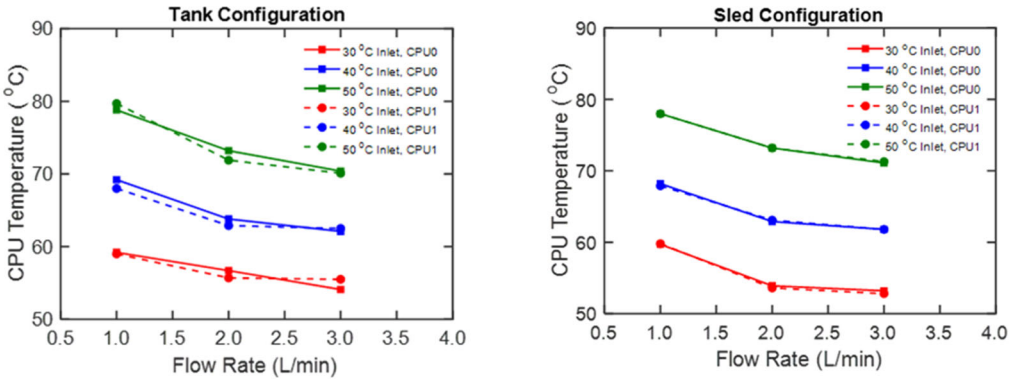


Figure 4-8 Results of tank-based and sled-based model simulations for different boundary conditions for CPU0 and CPU1

It can also be observed that the CPU peak temperature dropped with the decrease in the fluid inlet temperature. The change in the peak temperature is almost linear and approximately 10°C. Thermal shadowing was expected on the CPU1 as the fluid picks up heat from CPU0 and enters CPU1 heat sink with relatively higher temperature. But from the Figure 4-9, results observed at the bottom of the heatsink, it is observed that the relatively cold fluid on the side mixes with the hot fluid in the area between the heatsink 0 and 1 lowering the inlet temperature of the fluid entering heatsink 1. Thus, the temperatures of both the CPUs are comparable without thermal shadowing occurring.

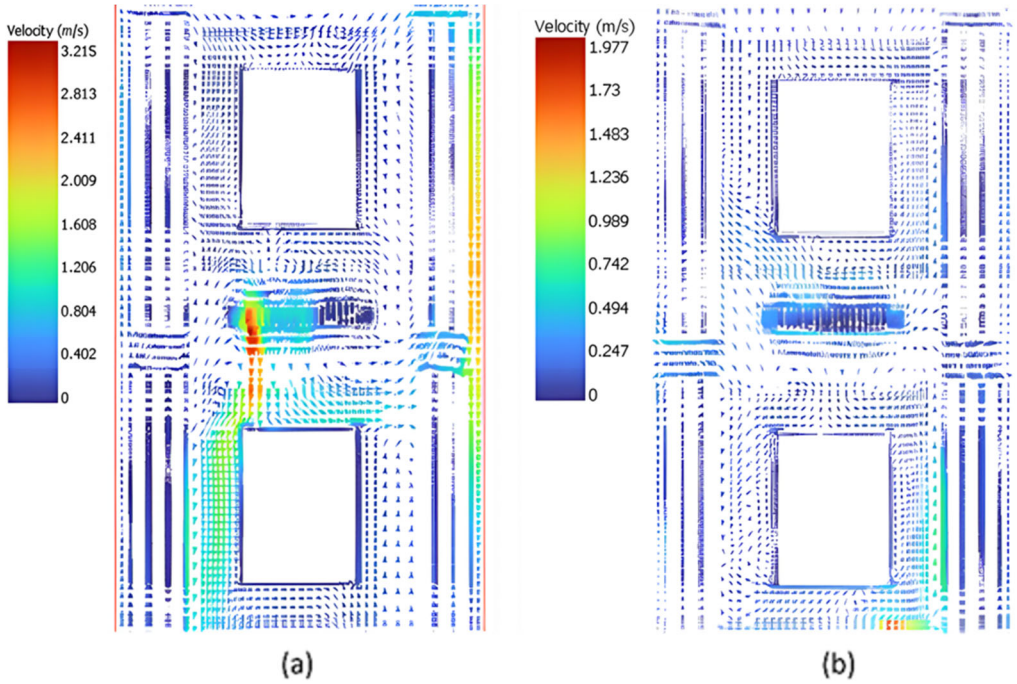


Figure 4-9 Flow mixing in the juncture between the two heatsinks in (a) tank configuration and (b) sled configuration for 30°C inlet temperature and 1 lpm flow rate.

The maximum allowed temperature of operation for HDD is 60°C. From Figure 4-10(a) and (b) it can be seen that all of the tank and sled configuration models operate within the expected range for all the flow rates and inlet temperatures except for the inlet temperature of 50°C. Though at higher flow rates, 50°C is keeping the HDD within operational temperature range, it would not be an ideal choice. Figure 4-10(c) and (d) show the peak temperatures among the DIMMs for tank and sled configurations respectively. The HDD and DIMM temperatures follow the same pattern as the CPUs for different inlet flows and temperatures. With the immersion cooling technology, the temperatures of all the components can be maintained below the maximum allowed temperature limits and

lower than the air-cooled technology, making immersion cooling efficient and promising than air cooling.

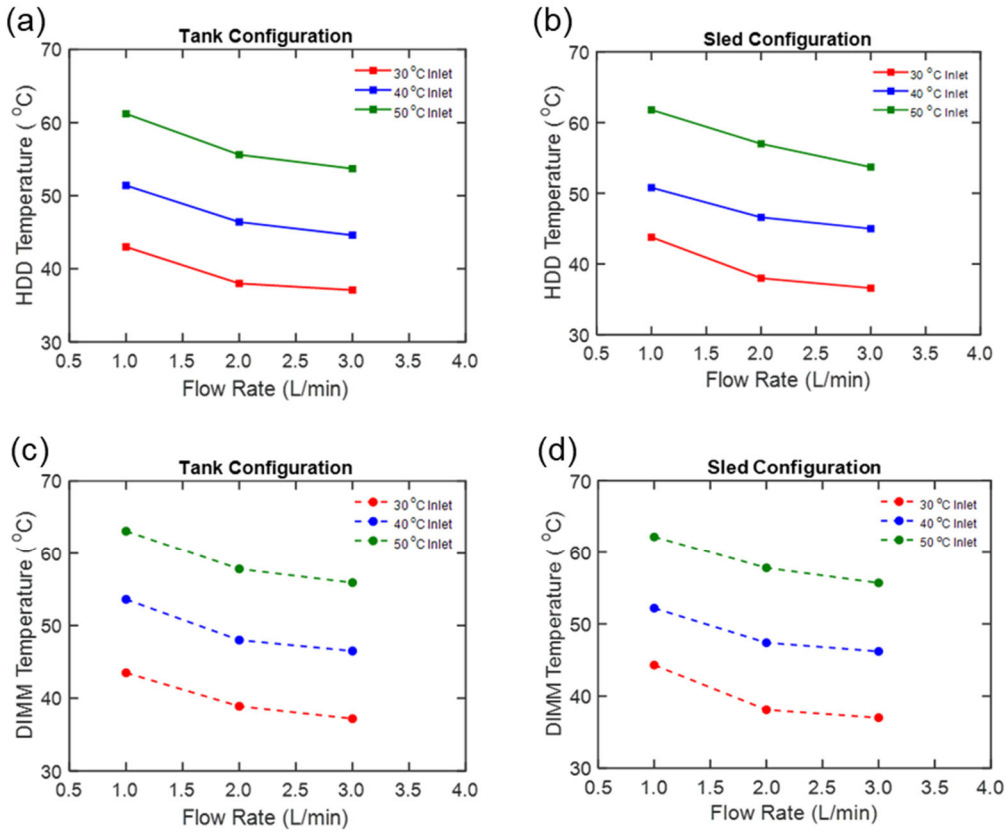


Figure 4-10 Results of (a) tank-based and (b) sled-based model simulations for different boundary conditions for HDD; and (c) tank-based and (d) sled-based model simulations for different boundary conditions for DIMM.

4.4 Conclusion

This study evaluated the feasibility of immersion cooling for a two-socket system that is designed for air-cooling. Analysis is performed for two configurations, tank and sled-based design. Temperature for CPUs, HDDs, DIMMs were studied under different operating conditions. The study shows that the sled design in which the server design is horizontal has the same performance as that of tank based immersion cooling solution. The analysis paves the way to design future immersion cooled servers in a form factor compatible to that of an air-cooled server. The sled-based design would require minimal infrastructure changes thus making it relatively easy to reap the benefits of immersion cooling technology. Future work includes optimization of the heat sink by virtue of which further gains could be realized.

Chapter 5

COOLING PERFORMANCE ENHANCEMENT OF IMMERSION COOLED TWO-SOCKET SERVER IN EC110 BASED NANOFLUID

5.1 Introduction to Nanofluids

Nanoparticles fall under a classification of advanced manufactured fluids, that comprise a base fluid like water, oil, ethylene glycol etc. The base fluids which is a dielectric are generally being predominantly used in immersion cooling of data center equipment. The nanoparticles can be metals, metal oxides, ceramics, or carbon-based particles and they are usually in the range of 1 to 100 nanometers in size. The nanoparticles have unique thermal, mechanical and optical properties. When these nanoparticles are combined with the base fluids, they enhance the properties of the fluids significantly, especially the thermal properties.

5.1.1 Benefits of Nanofluids for Immersion Cooling

When compared to the base fluid, the nanofluids exhibit significantly better thermal properties like thermal conduction. The addition of nanoparticles to the base fluid enhances the ability of the fluid to conduct and transfer heat. The enhancement of thermal properties in invaluable in applications like cooling system design for data centers, consumer electronics, heat exchangers and various cooling systems involved in industrial applications.

The increase in thermal conductivity translates into the fluids' ability to take away heat from the heat dissipating components of the packages. With the world progressing towards higher performances and clock speeds, there is an explosive increase in the heat dissipation from electronic packages. Modern electronics with high thermal dissipation

demand cooling solutions with higher heat absorption capacity. In industries like data centers, automotives, air conditioning where heat absorption rates for immersion fluids are required to be higher and efficient. Improved heat transfer efficiency of the cooling system can lead to better energy efficiency and overall system performance.

Nanofluids exhibit higher stability at higher temperatures when compared to conventional heat transfer fluids. This makes the nanofluids better suited for applications involving high thermal dissipations, such as in solar thermal systems, data centers and industrial processes where heat resistance is a critical factor.

The enhanced thermal conductivity leads to reduced temperature gradients within a server. Furthermore, the hotspots are tackled more efficiently compared to air cooling and immersion cooling with just the base fluid. It contributes to the overall stability and reliability of the immersed server systems.

With high thermal power of the CPUs and GPUs in the servers, the operating temperature of the base fluid is often raised closer to its boiling point. Nanofluids, with their enhanced thermal properties prevent the base fluid from boiling and changing phase from liquid to gas. Improved thermal properties also mean increased efficiency in the nanofluid and less pumping power required to circulate the fluid. Lower pumping power translates to higher energy efficiency of the entire circulating system. Energy efficiency of the system plays a crucial role in paving way to sustainable cooling solutions that have lower carbon footprint and greater positive impact on the environment along with being cost effective.

5.2 Single Phase Immersion Cooling Using Nanofluids

The single-phase immersion cooling of two socket shadow core server is expanded by employing Al_2O_3 nanoparticles. Al_2O_3 nanoparticles of size 80 nm are suspended in EC110 to make EC110/Al_2O_3 nanofluid. EC110/Al_2O_3 nanofluid based simulation is performed for the two-socket shadow core server configuration as described in Chapter 4. The Al_2O_3 nanoparticles properties are taken from literature. Table 5-1 represents the physical properties of Al_2O_3 nanoparticle[73].

The analysis is performed for three different mass fractions of nanoparticles in the base fluid: 0.01, 0.05, 0.1. The CPU junction temperature is taken as the measure to evaluate the efficiency of each mass fraction.

Table 5-1 Physical properties of Al_2O_3 nanoparticles

Physical Properties	Al_2O_3
Particle mean size (nm)	80
Specific heat Cp (J/KgK)	880
Density ρ (g/cc)	3.8
Conductivity λ (W/m-k)	40
Thermal diffusivity α × 107 (m2/s)	131.7
Thermal expansion ratio β (K−1 × 10−6)	8.5

5.3 Calculation of Effective Properties of Nanofluids

The effective properties of the EC110/Al_2O_3 nanofluid are calculated using the formulae from literature, represented in Figure 5-1. The effective properties of EC110/Al_2O_3 nanofluid are utilized to see how the peak temperatures of CPU 0 and CPU 1 are faring for the nanofluid in comparison to the base fluid for three different mass fractions chosen.

Effective thermal conductivity

$$\lambda_{\text{eff}} = \lambda_{\text{f}} \frac{[\lambda_{\text{p}}+(n-1)\lambda_{\text{f}}-(n-1)\phi_{\text{v}}(\lambda_{\text{f}}-\lambda_{\text{p}})]}{[\lambda_{\text{p}}+(n-1)\lambda_{\text{f}}+\phi_{\text{v}}(\lambda_{\text{f}}-\lambda_{\text{p}})]}$$

λ_f and λ_p are the thermal conductivity of the fluid and particles, respectively

n = 3 (spherical particles)

Volume fraction

$$\phi_{\text{v}} = \frac{\phi_{\text{w}}\rho_{\text{f}}}{\rho_{\text{p}}+\phi_{\text{w}}\rho_{\text{f}}-\phi_{\text{w}}\rho_{\text{p}}}$$

ρ_f and ρ_p are the density of the fluid and particles, respectively

ϕ_w is the mass fraction of the particles dispersed

Density

$$\rho_{\text{eff}} = \rho_{\text{p}}\phi_{\text{v}} + \rho_{\text{f}}(1-\phi_{\text{v}})$$

Diffusivity

$$\alpha_{\text{eff}} = \frac{\lambda_{\text{eff}}}{\rho_{\text{eff}}C_{\text{eff}}}$$

Specific Heat :

$$C_{\text{eff}} = C_{\text{p}}\phi_{\text{w}} + C_{\text{f}}(1-\phi_{\text{w}})$$

Suffix p for nanoparticles and f for base fluid

Figure 5-1 Formulae used for the calculation of thermal conductivity and other effective properties of nanofluids[74]

One important physical property enhancement the nanoparticles bring to the base fluid and thus the nanofluid is the enhancement in thermal conductivity. Figure 5-2 represents the effective thermal conductivity of the nanofluid for different mass fractions of nanoparticles.

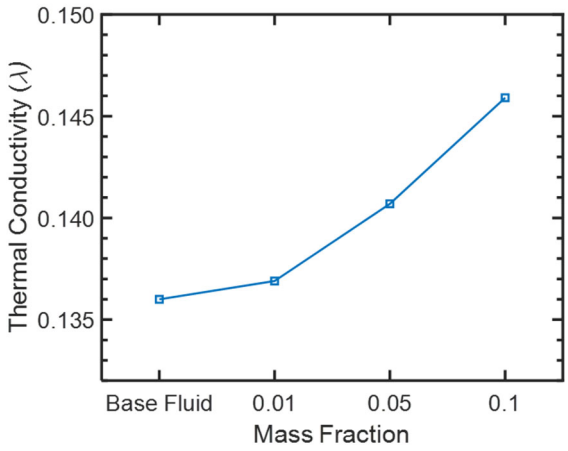


Figure 5-2 Effective thermal conductivity computed for base fluid and nanofluids with different mass fractions of nanoparticles.

Table 5-2 and Figure 5-3 represent the CPU0 and CPU1 junction temperatures with the under different mass fractions of Al_2O_3 nanoparticles in EC110 basefluid. From Figure 5-3 it is observed that the junction temperatures of CPU0 and CPU1 drop from base fluid, 0.01 and 0.5 mass fraction follows a linear trend. There is a steep decrease in CPU junction temperature from 0.05 mass fraction 0.1 mass fraction. Peak temperatures of CPU0 and CPU1 decrease with increase in mass fraction of nanoparticles in EC110/Al_2O_3 nanofluid and the peak temperature drop occurs between 0.05 and 0.1 mass fractions.

Table 5-2 Peak temperatures of CPU0 and CPU1 for various mass fractions of nanoparticles in EC110/Al_2O_3 nanofluid

Mass Fraction	CPU1	CPU0
Base Fluid	59.2	59
0.01	59.1	58.4
0.05	58.6	58.1
0.1	53.3	52.5

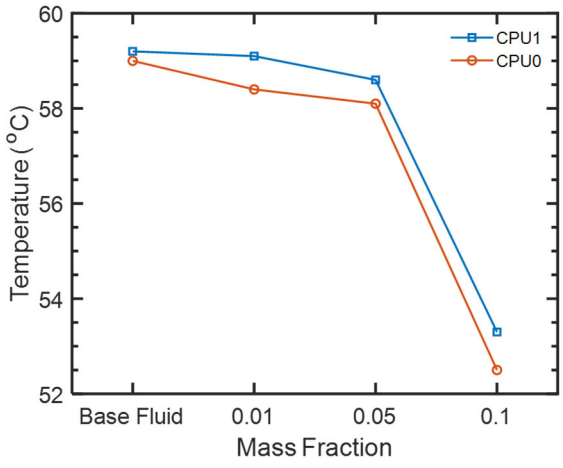


Figure 5-3 Peak temperatures of CPU0 and CPU1 for various mass fractions of nanoparticles in EC110/Al_2O_3 nanofluid

5.4 Conclusion

The effective properties of the EC110/Al_2O_3 nanofluid are calculated using the extensive literature and the derived formulae for effective properties of nanofluids when nanoparticles of 80 nm Al_2O_3 are suspended in EC110 nanofluids. It is observed that the nanoparticles enhance the thermal conductivity of the base fluid. The results show that the nanofluid efficiently reduced the thermal hotspots and CPU temperatures in comparison to the base fluid EC110.

Chapter 6

CONCLUDING REMARK AND FUTURE RESEARCH

The project “Challenges in co-packaging of Si-III/V components” explores the thermal and mechanical aspects of four interconnect designs—solder balls, flat pads, semi-annular, and annular designs—for the design of photonic integrated circuits. The solder interconnect design presented itself suitable for low current injection applications such as CMOS, the contact area becomes critical for high current injection applications, particularly in high-power photonic devices like lasers. With relatively large contact areas, the semi-annular and annular designs attain supremacy in electrical properties, as large contact reduces charge accumulation and lowers electrical resistance. Semi annular design offers multiple input output connections whereas annular interconnect design only allows one I/O connection per device. The semi annular design also works well in dissipating the heat from GaAs chip, almost equally as annular design. For the mechanical stress accumulation, semi annular design accumulates stress at the sharp corners of the interconnects. The mechanical stresses reduce significantly when the exterior corners are rounded.

For the glass interposer analysis project, the stress in the solder was relatively less affected by the thickness of the interposer and the stress decrease gradually with thickness and almost saturated at higher thicknesses. To avoid the higher processing using thicker interposer, 300 μm is an ideal thickness according to the study for the thickness range of 100 μm to 500 μm. For glass interposers, the thickness of the interposer had minimal effect on the stress on the substrate. Large solder ball did not take a lot of stress from the thickness difference from the interposer above it. The deformation in the glass

interposer decreased almost linearly with increase in the thickness. The stress at solder balls and copper/SiO2 interface decreases with increase in interposer thickness till 300 μm. Beyond that it saturates. Optimum thickness for glass interposer is 300 μm with 20 μm copper via diameter for the combination of glass interposer thicknesses and through package via diameters considered for the study.

This study on immersion cooling of two socket server in EC110 immersion fluid evaluated the feasibility of immersion cooling for a two-socket system that is designed for air-cooling in immersion cooling. Analysis is performed for two configurations, tank and sled- based design. Temperature for CPUs, HDDs, DIMMs were studied under different operating conditions. The study shows that the sled design in which the server design is horizontal has the same performance as that of tank based immersion cooling solution. The analysis paves the way to design future immersion cooled servers in a form factor compatible to that of an air-cooled server. The sled-based design would require minimal infrastructure changes thus making it relatively easy to reap the benefits of immersion cooling technology. EC110/Al_2O_3 nanofluid was employed to evaluate the CPU junction temperature reduction obtained by virtue of addition of nanoparticles to the base fluid. Future work includes optimization of the heat sink by virtue of which further gains could be realized.

This research work extends from chip level to server level in terms of reliability and thermal management. Further research in terms of flexible materials for packaging and nano-particles for the enhancement of thermal conductivity can drive the Silicon Photonics Glass Interposer Co-packaging and Nanofluids Immersion cooling technologies to revolutionize applications in terms of automation, 3D sensing, high density data storage and high-speed data transmission.

Appendix A

LIST OF PUBLICATIONS

1. **K Sivaraju**, R Bhandari, A Lakshminarayana, A Kalapala, G Gupta, P Bansode and D Agonafer, “Silicon Photonics Packages Interconnect Design and Analysis”, *The Intersociety Conference on Thermal And Thermomechanical Phenomena In Electronic Systems*, 2024 (Accepted)
2. **K Sivaraju**, R Bhandari, A Lakshminarayana, A Kalapala, G Gupta, P Bansode and D Agonafer, “Silicon Photonics Packages Design and Analysis”, *The Intersociety Conference on Thermal And Thermomechanical Phenomena In Electronic Systems*, 2024 (Accepted)
3. G Gupta, V Nair, A Pundla, P Bansode, **K Sivaraju** and D Agonafer, “Optimization Of A Heatsink Designed For Air Cooling For Immersion Cooling Application”, *International Electronic Packaging Technical Conference and Exhibition,* 2023
4. G Gupta, V Nair, A Pundla, P Bansode, **K Sivaraju** and D Agonafer, “A Numerical Study Comparing Forced And Natural Convection In A High-Density Single-Phase Immersed Cooled Server” *The Intersociety Conference on Thermal And Thermomechanical Phenomena In Electronic Systems*, 2023
5. A Sivakumar, A Barigala, V Simon, R Suthar, G Gupta**, K Sivaraju,** J Padilla, S Khalili, M Iyengar and D Agonafer “Investigation of heat sink design in a shadow core single-phase immersion cooled server”
6. **K Sivaraju**, P Bansode, G Gupta, J Lamotte-Dawaghreh, S Saini, , V Simon, J Herring, S Karajgikar, V Mulay, D Agonafer, “Comparative Study of Single-Phase Immersion Cooled Two Socket Server in Tank and Sled Configurations”, *International Electronic Packaging Technical Conference and Exhibition,* 2022
7. V Simon, H Modi, **K Sivaraju**, P Bansode, S Saini, P Shahi, S Karajgikar, V Mulay and D Agonafer, “Feasibility Study of Rear Door Heat Exchanger for a High Capacity Data Center”, *International Electronic Packaging Technical Conference and Exhibition,* 2022
8. R Bhandari, A Lakshminarayana, **K Sivaraju,** P Bansode, E.Keleja and D. Agonafer, “Impact of Immersion Cooling on Thermomechanical Properties of Non-Halogenated Substrate”, *International Electronic Packaging Technical Conference and Exhibition,* 2022
9. P Murthy, G Gupta, J Herring, J Lamotte-Dawaghreh, **K Sivaraju,** P Bansode, H Modi, P Mynapati, M Sweeney and D Agonafer “CFD Simulation-Based Comparative Study of Forced Convection Single-Phase Liquid Immersion Cooling for a High-Powered Server ”, *International Electronic Packaging Technical Conference and Exhibition,* 2022
10. T. Chauhan, R. Bhandari, **K Sivaraju**, R. Chowdhury and D. Agonafer, “Impact of immersion cooling on thermomechanical properties of low-loss material printed circuit boards”, *Journal of Enhanced Heat Transfer*, *28*(7), 2021
11. M. Kabir, R. Chowdhury, **K Sivaraju**, S. Dhandharphale, A. Lakshminarayan, S. Yadav and D. Agonafer “Enhancing the reliability of 3D package by analyzing crack behavior on TSV through structural optimization and comparing material properties of the package”, *SMTA International Conference*, 2020

12. T. Chauhan, A. Misrak, R. Bhandari, P. Rajmane, R. Chowdhury, **K. Sivaraju**, M. Abdulhasansari and D. Agonafer, “Impact of Thermal Aging and Cycling on Reliability of Thermal Interface Materials”, *SMTA International Conference*, 2019

References

[1] A. Kalapala *et al.*, “Impact of Cavity Resonance Detuning on Watt-Level PCSELs,” in *2022 IEEE Photonics Conference (IPC)*, 2022, pp. 1–2. doi: 10.1109/IPC53466.2022.9975563.

[2] A. Y. Song, A. R. K. Kalapala, W. Zhou, and S. Fan, “First-principles simulation of photonic crystal surface-emitting lasers using rigorous coupled wave analysis,” *Appl Phys Lett*, vol. 113, no. 4, p. 041106, Jul. 2018, doi: 10.1063/1.5045486.

[3] M. Zhou *et al.*, “Increasing the Q-Contrast in Large Photonic Crystal Slab Resonators Using Bound-States-in-Continuum,” *ACS Photonics*, vol. 10, no. 5, pp. 1519–1528, May 2023, doi: 10.1021/acsphotonics.3c00126.

[4] D. Liu *et al.*, “226 nm AlGaN/AlN UV LEDs using p-type Si for hole injection and UV reflection,” *Appl Phys Lett*, vol. 113, no. 1, p. 011111, Jul. 2018, doi: 10.1063/1.5038044.

[5] C. Reuterskiöld Hedlund, J. Martins De Pina, A. Kalapala, Z. Liu, W. Zhou, and M. Hammar, “Buried InP/Airhole Photonic-Crystal Surface-Emitting Lasers,” *physica status solidi (a)*, vol. 218, no. 3, p. 2000416, Feb. 2021, doi: https://doi.org/10.1002/pssa.202000416.

[6] D. Liu *et al.*, “Influences of screw dislocations on electroluminescence of AlGaN/AlN-based UVC LEDs,” *AIP Adv*, vol. 9, no. 8, p. 085128, Aug. 2019, doi: 10.1063/1.5108743.

[7] G. Fish, J. Roth, V. Kaman, and A. Fang, “Advances in III–V heterogeneous integration on silicon,” in *IEEE Photonics Conference 2012*, 2012, pp. 747–748. doi: 10.1109/IPCon.2012.6358838.

[8] A. R. K. Kalapala, C. Guo, L. Overman, M. Vasilyev, J. Coleman, and W. Zhou, “Linewidth and Cavity Feedback in Photonic Crystal Surface Emitting Lasers,” in *2021 IEEE Photonics Conference (IPC)*, 2021, pp. 1–2. doi: 10.1109/IPC48725.2021.9593049.

[9] A. Kalapala *et al.*, “Scaling Challenges in High Power Photonic Crystal Surface-Emitting Lasers,” *IEEE J Quantum Electron*, vol. 58, no. 4, pp. 1–9, 2022, doi: 10.1109/JQE.2022.3165314.

[10] B. M. D. Sawyer *et al.*, “Design and Demonstration of a 2.5-D Glass Interposer BGA Package for High Bandwidth and Low Cost,” *IEEE Trans Compon Packaging Manuf Technol*, vol. 7, no. 4, pp. 552–562, 2017, doi: 10.1109/TCPMT.2017.2659700.

[11] K. B. Sivaraju *et al.*, “Comparitive study of two socket,” *International Electronic Packaging Technical Conference and Exhibition*, 2022, doi: https://doi.org/10.1115/IPACK2022-97429.

[12] B. Jalali and S. Fathpour, “Silicon Photonics,” *Journal of Lightwave Technology*, vol. 24, no. 12, pp. 4600–4615, 2006, doi: 10.1109/JLT.2006.885782.

[13] M. Kim *et al.*, “Nanoscale groove textured β-Ga2O3 by room temperature inverse metal-assisted chemical etching and photodiodes with enhanced responsivity,” *Appl Phys Lett*, vol. 113, no. 22, p. 222104, Nov. 2018, doi: 10.1063/1.5053219.

[14] A. R. K. Kalapala *et al.*, “Optically pumped room temperature low threshold deep UV lasers grown on native AlN substrates,” in *Proc.SPIE*, Mar. 2019, p. 109180I. doi: 10.1117/12.2508717.

[15] K. J. Reilly *et al.*, “Fabrication Methods for Photonic Crystal Surface Emitting Lasers (PCSELs) by Molecular Beam Epitaxy,” in *2022 Compound*

Semiconductor Week (CSW), 2022, pp. 1–2. doi: 10.1109/CSW55288.2022.9930418.

[16] A. Y. Song *et al.*, “Controllable finite ultra-narrow quality-factor peak in a perturbed Dirac-cone band structure of a photonic-crystal slab,” *Appl Phys Lett*, vol. 119, no. 3, p. 031105, Jul. 2021, doi: 10.1063/5.0056243.

[17] A. R. K. Kalapala *et al.*, “Optically Pumped 1 μm Low Threshold Photonic Crystal Surface Emitting Lasers Grown on GaAs Substrate,” in *2019 IEEE Photonics Conference (IPC)*, 2019, pp. 1–2. doi: 10.1109/IPCon.2019.8908472.

[18] E. Amador *et al.*, “A new pyridinium-substituted tetraphenylethylene aggregation induced emission composites for rare-earth free white light displays,” *Materials Today Physics*, vol. 33, p. 101036, 2023, doi: https://doi.org/10.1016/j.mtphys.2023.101036.

[19] M. Pan, Z. Liu, A. R. K. Kalapala, Y. Chen, Y. Sun, and W. Zhou, “Complete 2π phase control by photonic crystal slabs,” *Opt Express*, vol. 29, no. 25, pp. 40795–40803, 2021, doi: 10.1364/OE.440687.

[20] K. Das and A. Kalapala, “Spectral Properties of Glare or Positive Dysphotopsia for Different Types of Intraocular Lenses,” *Invest Ophthalmol Vis Sci*, vol. 62, no. 8, p. 496, Jun. 2021.

[21] A. Y. Song, A. R. K. Kalapala, W. Zhou, and S. Fan, “First-principles simulation of photonic-crystal surface-emitting lasers using rigorous coupled wave analysis (Conference Presentation),” in *Proc.SPIE*, Mar. 2019, p. 1093908. doi: 10.1117/12.2508690.

[22] L.-D. Yuan, H.-X. Deng, S.-S. Li, S.-H. Wei, and J.-W. Luo, “Unified theory of direct or indirect band-gap nature of conventional semiconductors,” *Phys Rev B*, vol. 98, no. 24, p. 245203, Dec. 2018, doi: 10.1103/PhysRevB.98.245203.

[23] K. J. Reilly *et al.*, “Epitaxial Regrowth and Hole Shape Engineering for Photonic Crystal Surface Emitting Lasers (PCSELs),” *J Cryst Growth*, vol. 535, p. 125531, 2020, doi: https://doi.org/10.1016/j.jcrysgro.2020.125531.

[24] K. K. Das and A. R. Kalapala, “Assessment of spectral properties of positive dysphotopsia or glare caused by LED sources for different types of intraocular lenses,” *Opt Express*, vol. 30, no. 15, pp. 27140–27148, 2022, doi: 10.1364/OE.465822.

[25] “Book Reviews,” *Journal of the Optical Society of America A*, vol. 3, no. 3, pp. 378–379, 1986, doi: 10.1364/JOSAA.3.000378.

[26] K. J. Reilly *et al.*, “Fabrication of Photonic Crystal Surface Emitting Lasers (PCSELs) by Epitaxial Regrowth,” in *Conference on Lasers and Electro-Optics*, J. Kang Tomasulo S. Ilev I. Müller D. Litchinitser N. Polyakov S. Podolskiy V. Nunn J. Dorrer C. Fortier T. Gan Q. and Saraceno C., Ed., in OSA Technical Digest. San Jose, California: Optica Publishing Group, 2021, p. JTu3A.78. [Online]. Available: https://opg.optica.org/abstract.cfm?URI=CLEO_QELS-2021-JTu3A.78

[27] J. H. Lau *et al.*, “Design and analysis of 3D stacked optoelectronics on optical printed circuit boards,” in *Proc.SPIE*, Feb. 2008, p. 689907. doi: 10.1117/12.764032.

[28] L. Sirleto and G. Righini, “An Introduction to Nonlinear Integrated Photonics Structures and Devices micromachines,” *Micromachines (Basel)*, vol. 14, no. 3, 2023, doi: https://doi.org/10.3390/mi14030614.

[29] M. Kabir, A. R. Chowdhury, K. B. Sivaraju, S. Dhandarphale, and D. Agonafer, “Enhancing the crack behaviour scholar,” *SMTA International*, 2020.

[30] T. Komljenovic, D. Huang, P. Pintus, M. A. Tran, M. L. Davenport, and J. E. Bowers, “Photonic Integrated Circuits Using Heterogeneous Integration on

Silicon," *Proceedings of the IEEE*, vol. 106, no. 12, pp. 2246–2257, 2018, doi: 10.1109/JPROC.2018.2864668.
[31] N. C. Abrams *et al.*, "Silicon Photonic 2.5D Multi-Chip Module Transceiver for High-Performance Data Centers," *Journal of Lightwave Technology*, vol. 38, pp. 3346–3357, 2020, [Online]. Available: https://api.semanticscholar.org/CorpusID:211480608
[32] C.-C. Liu, Y.-K. Lin, M.-P. Houng, and Y.-H. Wang, "The microstructure investigation of flip-chip laser diode bonding on silicon substrate by using indium-gold solder," *IEEE Transactions on Components and Packaging Technologies*, vol. 26, no. 3, pp. 635–641, 2003, doi: 10.1109/TCAPT.2003.817655.
[33] B. M. D. Sawyer *et al.*, "Design and Demonstration of a 2.5-D Glass Interposer BGA Package for High Bandwidth and Low Cost," *IEEE Trans Compon Packaging Manuf Technol*, vol. 7, no. 4, pp. 552–562, 2017, doi: 10.1109/TCPMT.2017.2659700.
[34] A. Elshabini, G. Wang, and F. Barlow, "Future trends in electronic packaging," in *Proc.SPIE*, Mar. 2006, p. 61720Z. doi: 10.1117/12.668750.
[35] X. Qin *et al.*, "Large silicon, glass and low CTE organic interposers to printed wiring board SMT interconnections using copper microwire arrays," in *2013 IEEE 63rd Electronic Components and Technology Conference*, 2013, pp. 867–871. doi: 10.1109/ECTC.2013.6575675.
[36] B. Bayraktaroglu, "Heterogeneous Integration Technology," May 2017.
[37] D.-C. Hu, Y.-P. Hung, Y. H. Chen, R.-M. Tain, and W.-C. Lo, "Embedded glass interposer for heterogeneous multi-chip integration," in *2015 IEEE 65th Electronic Components and Technology Conference (ECTC)*, 2015, pp. 314–317. doi: 10.1109/ECTC.2015.7159610.
[38] G. Fish, J. Roth, V. Kaman, and A. Fang, "Advances in III–V heterogeneous integration on silicon," in *IEEE Photonics Conference 2012*, 2012, pp. 747–748. doi: 10.1109/IPCon.2012.6358838.
[39] S. Crouse, "Challenges in Predicting Thermal Integrity of 2.5D and 3D-ICs," Linkedin.com/Abachy.
[40] B. M. D. Sawyer *et al.*, "Design and Demonstration of a 2.5-D Glass Interposer BGA Package for High Bandwidth and Low Cost," *IEEE Trans Compon Packaging Manuf Technol*, vol. 7, no. 4, pp. 552–562, 2017, doi: 10.1109/TCPMT.2017.2659700.
[41] C.-H. Chien *et al.*, "Performance and process characteristic of glass interposer with through-glass-via(TGV)," in *2013 IEEE International 3D Systems Integration Conference (3DIC)*, 2013, pp. 1–7. doi: 10.1109/3DIC.2013.6702380.
[42] S. Cho, Y. Joshi, V. Sundaram, Y. Sato, and R. Tummala, "Comparison of thermal performance between glass and silicon interposers," in *2013 IEEE 63rd Electronic Components and Technology Conference*, 2013, pp. 1480–1487. doi: 10.1109/ECTC.2013.6575767.
[43] M. Töpper *et al.*, "3-D Thin film interposer based on TGV (Through Glass Vias): An alternative to Si-interposer," in *2010 Proceedings 60th Electronic Components and Technology Conference (ECTC)*, 2010, pp. 66–73. doi: 10.1109/ECTC.2010.5490887.
[44] H. Lee *et al.*, "Electrical characterization of bump-less high speed channel on silicon, organic and glass interposer," in *2014 IEEE International Symposium on Electromagnetic Compatibility (EMC)*, 2014, pp. 850–854. doi: 10.1109/ISEMC.2014.6899086.

[45] A. Usman *et al.*, “Interposer Technologies for High-Performance Applications,” *IEEE Trans Compon Packaging Manuf Technol*, vol. 7, no. 6, pp. 819–828, 2017, doi: 10.1109/TCPMT.2017.2674686.
[46] J. Kim *et al.*, “Silicon vs. Organic Interposer: PPA and Reliability Tradeoffs in Heterogeneous 2.5D Chiplet Integration,” in *2020 IEEE 38th International Conference on Computer Design (ICCD)*, 2020, pp. 80–87. doi: 10.1109/ICCD50377.2020.00030.
[47] C.-H. Chien *et al.*, “Performance and Process Comparison between Glass and Si Interposer for 3D-IC Integration,” *International Symposium on Microelectronics*, vol. 2013, no. 1, pp. 618–624, Jan. 2013, doi: 10.4071/isom-2013-WP12.
[48] Y.-H. Chen *et al.*, “Low Cost Glass Interposer Development,” *International Symposium on Microelectronics*, vol. 2014, no. 1, pp. 397–401, Oct. 2014, doi: 10.4071/isom-WA15.
[49] G. Kumar, T. Bandyopadhyay, V. Sukumaran, V. Sundaram, S. K. Lim, and R. Tummala, “Ultra-high I/O density glass/silicon interposers for high bandwidth smart mobile applications,” in *2011 IEEE 61st Electronic Components and Technology Conference (ECTC)*, 2011, pp. 217–223. doi: 10.1109/ECTC.2011.5898516.
[50] S. Kuramochi, H. Kudo, M. Akazawa, H. Mawatari, M. Tanaka, and Y. Fukuoka, “Glass interposer technology advances for high density packaging,” in *2016 IEEE CPMT Symposium Japan (ICSJ)*, 2016, pp. 213–216. doi: 10.1109/ICSJ.2016.7801263.
[51] J. H. Lau, *Heterogeneous integrations*. Springer, 2019.
[52] J. H. Lau *et al.*, “Through-Silicon Hole Interposers for 3-D IC Integration,” *IEEE Trans Compon Packaging Manuf Technol*, vol. 4, no. 9, pp. 1407–1419, 2014, doi: 10.1109/TCPMT.2014.2339832.
[53] C.-H. Chien *et al.*, “Performance and process characteristic of glass interposer with through-glass-via(TGV),” in *2013 IEEE International 3D Systems Integration Conference (3DIC)*, 2013, pp. 1–7. doi: 10.1109/3DIC.2013.6702380.
[54] C. Nadjahi, H. Louahlia, and S. Lemasson, “A review of thermal management and innovative cooling strategies for data center,” *Sustainable Computing: Informatics and Systems*, vol. 19, pp. 14–28, Sep. 2018, doi: 10.1016/J.SUSCOM.2018.05.002.
[55] R. Bhandari, A. B. Lakshminarayana, K. B. Sivaraju, P. Bansode, E. Kejela, and D. Agonafer, “Impact of Immersion Cooling on Thermomechanical Properties of Non-Halogenated Substrate citations-20231218T063917,” *International Electronic Packaging Technical Conference and Exhibition*, 2022, doi: https://doi.org/10.1115/IPACK2022-97423.
[56] K. Ebrahimi, G. F. Jones, and A. S. Fleischer, “A review of data center cooling technology, operating conditions and the corresponding low-grade waste heat recovery opportunities,” *Renewable and Sustainable Energy Reviews*, vol. 31, pp. 622–638, Mar. 2014, doi: 10.1016/J.RSER.2013.12.007.
[57] V. S. Simon *et al.*, “Energy Analysis of Rear Door Heat Exchangers in Data Centers With Spatial Workload Distribution citations-20231218T064801,” *International Electronic Packaging Technical Conference and Exhibition*, 2023, doi: https://doi.org/10.1115/IPACK2023-112078.
[58] V. S. Simon *et al.*, “Feasibility Study of Rear Door Heat Exchanger for a High Capacity Data Center citations-20231218T060810,” *International Electronic Packaging Technical Conferernce and Exhibition*, 2022, doi: https://doi.org/10.1115/IPACK2022-97494.

[59] T. Chauhan, R. Bhandari, K. B. Sivaraju, A. S. M. R. Chowdhury, and D. Agonafer, “Impact of Immersion Cooling on Thermomechanical Properties of Low-Loss Material Printed Circuit Boards scholar,” *Journal of Enhanced Heat Transfer*, vol. 28, no. 7, pp. 73–90, 2021, doi: 10.1615/JEnhHeatTransf.2021039486.
[60] T. Chauhan *et al.*, “Impact of thermal aging and cycling on reliability of thermal interface materials scholar,” *Proceedings of SMTA International*, pp. 118–123, 2019.
[61] P. Murthy *et al.*, “CFD Simulation-Based Comparative Study of Forced Convection Single-Phase Liquid Immersion Cooling for a High-Powered Server citations-20231218T062306,” *International Electronic Packaging Technical Conference and Exhibition*, 2022, doi: https://doi.org/10.1115/IPACK2022-97402.
[62] G. Gupta *et al.*, “A Numerical Study Comparing Forced and Natural Convection in a High-Density Single-Phase Immersed Cooled Serve citations-20231218T065021,” *International Electronic Packaging Technical Conference and Exhibition*, 2023, doi: https://doi.org/10.1115/IPACK2023-112065.
[63] P. E. Tuma, “The merits of open bath immersion cooling of datacom equipment,” in *Annual IEEE Semiconductor Thermal Measurement and Management Symposium*, 2010, pp. 123–131. doi: 10.1109/STHERM.2010.5444305.
[64] P. Bansode *et al.*, “Impact of Immersion Cooling on Thermomechanical Properties of Halogen-Free Substrate Core citations-20231218T064450,” *International Electronic Packaging Technical Conference and Exhibition*, 2023, doi: https://doi.org/10.1115/IPACK2023-111056.
[65] Q. Liu, Y. Ma, M. Alhussein, Y. Zhang, and L. Peng, “Green data center with IoT sensing and cloud-assisted smart temperature control system,” *Computer Networks*, vol. 101, pp. 104–112, Jun. 2016, doi: 10.1016/j.comnet.2015.11.024.
[66] P. V Bansode *et al.*, “MEASUREMENT OF THE THERMAL PERFORMANCE OF A SINGLE-PHASE IMMERSION COOLED SERVER AT ELEVATED TEMPERATURES FOR PROLONGED TIME,” 2018. [Online]. Available: https://proceedings.asmedigitalcollection.asme.org
[67] V. S. Simon *et al.*, “Feasibility study scholar,” *International Electronic Packaging Technical Conference and Exhibition*, vol. 86557, p. V001T01A018, Oct. 2022.
[68] R. Eiland, J. Fernandes, M. Vallejo, D. Agonafer, and V. Mulay, “Flow Rate and inlet temperature considerations for direct immersion of a single server in mineral oil,” in *Thermomechanical Phenomena in Electronic Systems -Proceedings of the Intersociety Conference*, Institute of Electrical and Electronics Engineers Inc., Sep. 2014, pp. 706–714. doi: 10.1109/ITHERM.2014.6892350.
[69] A. C. Kheirabadi and D. Groulx, “Cooling of server electronics: A design review of existing technology,” *Applied Thermal Engineering*, vol. 105. Elsevier Ltd, pp. 622–638, Jul. 25, 2016. doi: 10.1016/j.applthermaleng.2016.03.056.
[70] G. Gupta *et al.*, “Optimization of a Air-Cooled Heatsink for Immersion Cooling Application citations-20231218T064124,” *International Electronic Packaging Technical Conference and Exhibition*, 2023, doi: https://doi.org/10.1115/IPACK2023-112054.
[71] W. Zhao and J. Ning, “Open Compute Project FB 2S Server Tioga Pass,” *Facebook Open Compute Project*, 2020.
[72] H. Coles and M. Herrlin, “Immersion Cooling of Electronics in DoD Installations Distribution Statement A,” 2016.
[73] M. Corcione, “Empirical correlating equations for predicting the effective thermal conductivity and dynamic viscosity of nanofluids,” *Energy Convers Manag*, vol. 52, no. 1, pp. 789–793, 2011, doi: https://doi.org/10.1016/j.enconman.2010.06.072.

[74] X. Zhang, H. Gu, and M. Fujii, “Effective thermal conductivity and thermal diffusivity of nanofluids containing spherical and cylindrical nanoparticles,” *Exp Therm Fluid Sci*, vol. 31, no. 6, pp. 593–599, 2007, doi: https://doi.org/10.1016/j.expthermflusci.2006.06.009.

Biographical Information

Krishna Bhavana Sivaraju was born in Ongole, Andhra Pradesh, India. She received Bachelor's degree in 2016 from Rajiv Gandhi University of Knowledge Technologies, specializing in Mechanical Engineering. During her undergrad studies, she participated in various research activities and competitions including space solar power satellite design conducted by NASA and Ohio University in 2014.

In Spring 2019, Krishna Bhavana joined Dr. Agonafer's Electronics, MEMS and Nano Technology Systems Packaging Center group at University of Texas at Arlington as a PhD candidate. Her research interests include design, fabrication and thermos-mechanical testing of electronic packaging systems. Her area of expertise includes III-V/Si Photonics co-packing technology for high-speed data transmission and efficient thermal, mechanical and electrical performance. She worked on testing glass as interposer material for 3D packaging where through glass via geometry is optimized to understand how different packaging co depend on each other in terms of material, geometry and placement. She contributed towards immersion cooling design of servers for efficient thermal performance. She proposed and studied a new horizontal sled configuration and assessed its performance against the traditional tank configuration of liquid immersion cooling. She extended the study towards nanofluids to evaluate thermal performance gain provided by the addition of nanoparticles to the base fluid.

Prior to joining UTA, Krishna Bhavana worked as Jr. Mechanical Engineer at IMEG Corp., India developing thermal solutions to advanced infrastructural developments including research facilities and clean rooms. During her time at UTA she worked as course instructor for courses Fundamentals in Electronic Packaging and Computational Techniques for Electronic Packaging. She is the recipient of best paper award at ASME InterPACK 2022. She received grand first prize for her design of space solar power satellite

in International SunSat Design Competition, 2014. She attended multiple international conferences and served as reviewer to various peer reviewed journals. Krishna Bhavana plans to pursue a career in design, development and fabrication of novel electronic packaging components.